

Tutorials & Workshops



Université
de Toulouse

Introduction to the modeling and simulation of electromagnetic compatibility of integrated circuits

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www.ic-emc.org

12th April 2010, 9.00 am – 5.30 pm

Outlines

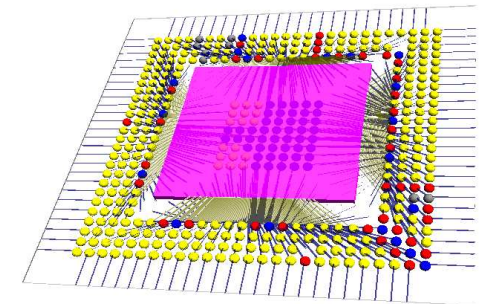
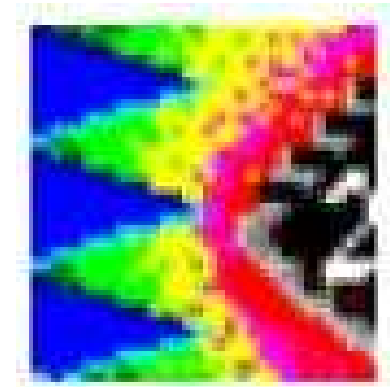
- **AGENDA**
 - Morning : 9.00 am – 12.00 am: Exercises on basic notions for EMC of ICs
 - Afternoon: 2.00 pm – 5.30 pm: Advanced problems
- **OBJECTIVES**
 - At the end of the course, the auditor will be able to understand the basic concepts associated to EMC at IC level and build simple models to evaluate the emission and the susceptibility of circuits.
- **PRE REQUISITES**
 - Basic knowledge in CMOS technology, MOS models and electromagnetic compatibility
 - Basic experience with SPICE simulator

Outlines

- **Covered topics**
 - IC transient current estimation
 - Conducted emission simulation
 - IC emission modeling (ICEM)
 - IC, Package and PCB interconnects
 - IC conducted susceptibility
 - RFI induced offset (rectification)
 - On-chip decoupling evaluation and budget
 - Modeling of EMC measurement set-up for ICs

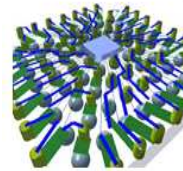
IC-EMC

- All the notions will be illustrated with IC-EMC
 - IC-EMC is a friendly and free PC tool for modeling and simulating EMC at IC level.
 - The tool is linked with the shareware WinSPICE derived from SPICE Berkeley for analog simulation (www.winspice.com)
 - Download IC-EMC and the user manual <http://www.ic-emc.org>
 - Version used for the training: IC-EMC 2.1



Getting started

- <http://www.ic-emc.org>
- Download the package icemc.zip
- Unzip in “C:/TEMP”
- Open “/system”, double click “ic-emc.exe” to launch IC-EMC



Welcome to IC-EMC homepage

The IC-EMC software is the non-commercial tool to illustrate the electromagnetic compatibility (EMC) circuits (IC). The tool has been developed within the frame of the European projects [MEDEA+](#) Paracl "EmcPack" and [Aerospace-Valley](#) project "EPEA".

The software has been developed by [Etienne SICARD](#) and [Alexandre BOYER](#), [INSA-Toulouse](#), France, their research on [EMC of ICs](#) at [LATTIS](#) labs.

New! : Version 2.0 available for FREE NOW ([download...](#)), with a completely new 300 pp documentation ([download...](#))

New! : Half-day tutorial IC-EMC at [AP EMC Beijing](#), April 2010 ([more information...](#))

New! : [Demonstration](#) at EMC Compo 09, November 2009 ([more information...](#))

New! *Version 2.0 user's manual version* now available for download!

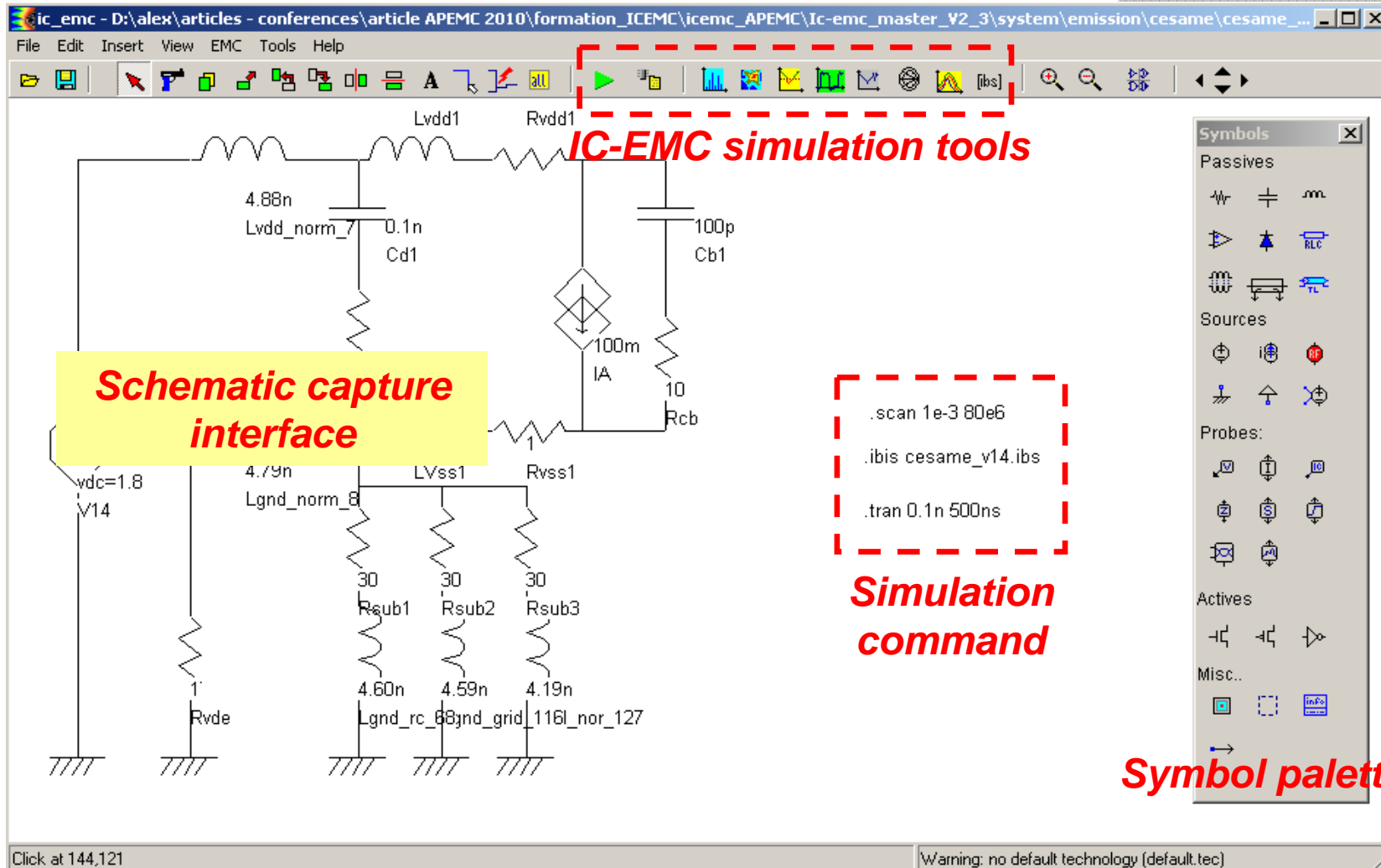
Download

New!

- [N port](#)
- [Automatic susceptibility extraction](#)



IC-EMC main screen

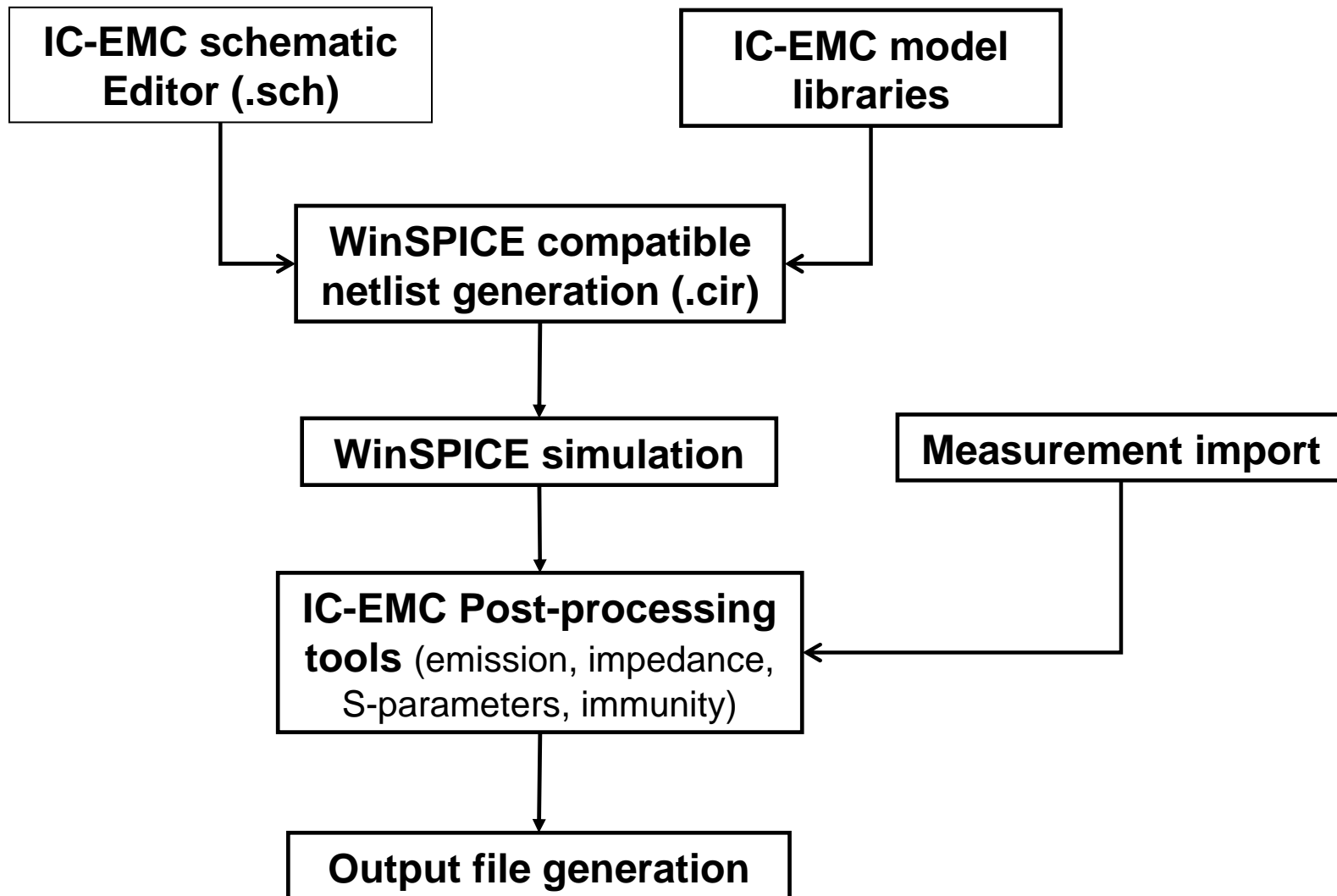


The screenshot displays the IC-EMC software interface. The main window shows a circuit schematic with various components and their values. A red dashed box highlights the simulation tools toolbar, labeled "IC-EMC simulation tools". A yellow box highlights the schematic capture interface, labeled "Schematic capture interface". A red dashed box highlights the simulation command window, labeled "Simulation command", containing the following commands:























```
.scan 1e-3 80e6
.ibis cesame_v14.ibs
.tran 0.1n 500ns
```

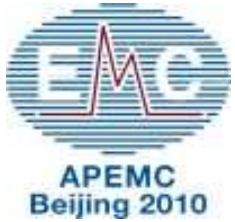
A red dashed box highlights the symbol palette, labeled "Symbol palette". The status bar at the bottom shows "Click at 144,121" and "Warning: no default technology (default.tec)".

IC-EMC Simulation flow



Most important icons

	Open schematic (.sch)		Build SPICE netlist (.cir)
	Save schematic (.sch)		Spectrum analysis
	Delete symbols		Near field emission simu.
	Copy symbols		Immunity simulation
	Move symbols		Time domain analysis
	Rotate symbols		Impedance simulation
	Flip symbols		S parameter simulation
	Add Text line		Ibis file editor
	Add a line		Parametric analysis
	View electrical net		Symbol palette
	Insert library file (.lib)		View all schematic



WinSPICE simulation

- Click on WinSPICE.exe
- Click File/Open to open a circuit netlist (.cir) generated by ic-emc.
- IC-EMC main commands (text line):

```
WinSpice v1.05.01
File Edit Settings Help
*****
WinSpice © Copyright 1996-2003 OuseTech Ltd. All Rights Reserved.
Version: 1.05.01
Built : Dec 10 2003 00:47:53
Shareware version of WinSpice. For non-commercial use only.
Please read the file 'license.txt' for conditions of use.
*****
Type "help" for more information, "quit" to leave.
WinSpice 1 -> _
```

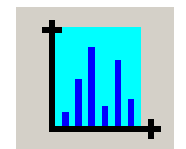
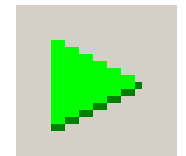
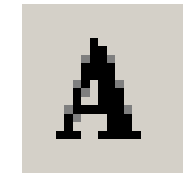
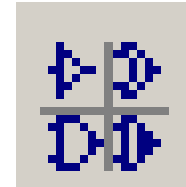
Simulation command	Command line	Parameters
Transient simulation	.tran 0.1n 100n	step + stop time
DC simulation	.DC Vdd 0 5 0.1	source + start + stop + step
Small signal freq. analysis	.AC DEC 100 1MEG 1G	sampling + nb points + start + stop

I. Exercises

- Basic notions for EMC of IC modeling presented through the following exercises:
 - Ex 1. FFT of typical signals
 - Ex 2. IC transient current estimation
 - Ex 3. Interconnect parasitics
 - Ex 4. di/dt noise
 - Ex 5. On-chip decoupling
 - Ex 6. Estimation of susceptibility level
 - Ex 7. Immunity of an output buffer

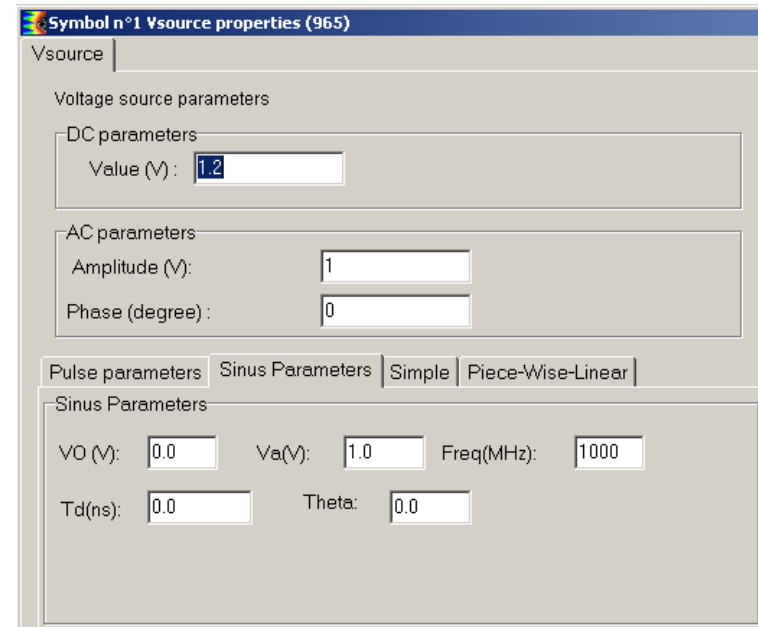
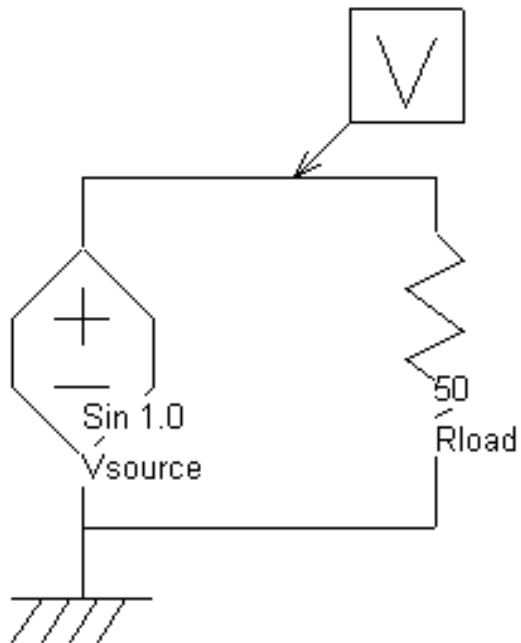
I. Exercises

- Exercise 1. FFT of typical signals
 - Create the schematic
 - Set the source generator
 - Transient simulation
 - FFT by IC-EMC
 - Simulate the FFT of a sinus and a square signal





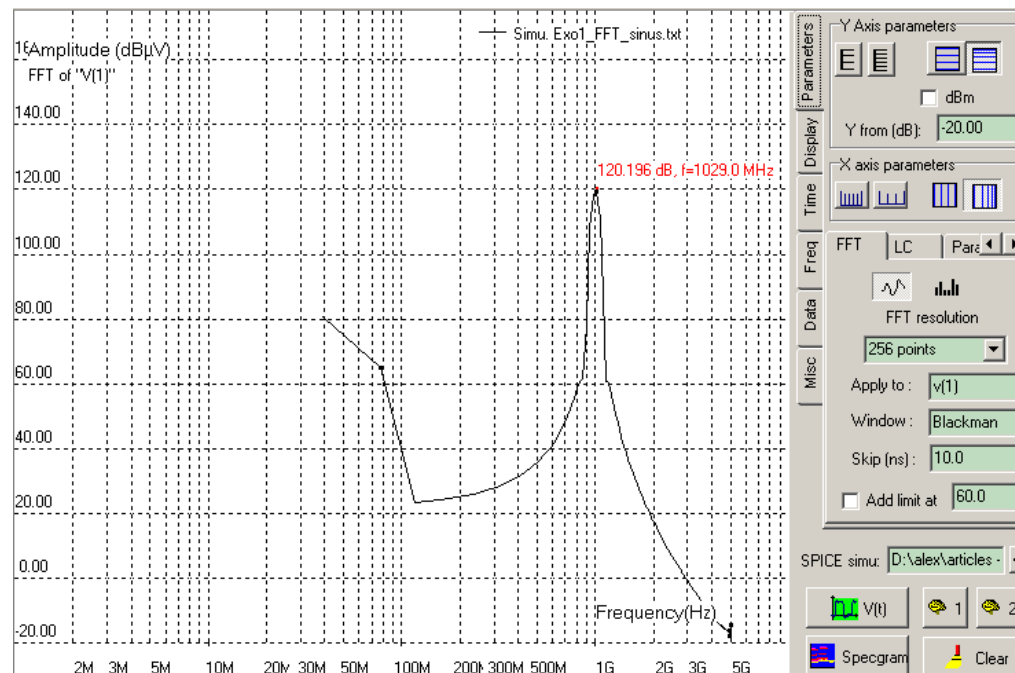
I. Exercises

- FFT of a sinus source
 - Set the voltage generator properties:
 - Frequency = 1 GHz
 - Amplitude = 1 V



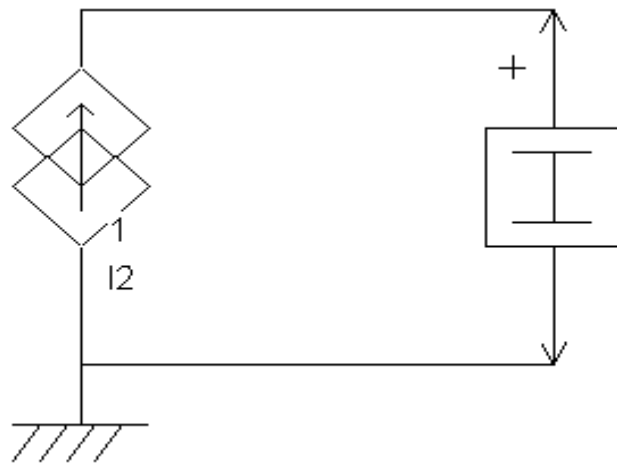
I. Exercises

- FFT of a sinus source
 - Type the simulation command: `.tran 1n 50n`
 - Simulate the response in time domain. 
 - Compute the FFT. 
 - Does the FFT result correlate with theoretical result ?



I. Exercises

- FFT of a square source
 - Set the generator properties to :
 - Period = 10 n,
 - PW = 4 n,
 - Tr = 1n, Tf = 1 n
 - I0 = 0 A, I1 = 1 A



.tran 0.1n 500n

Pulse parameters | Sinus Parameters | Simple | Piece-Wise-Linear

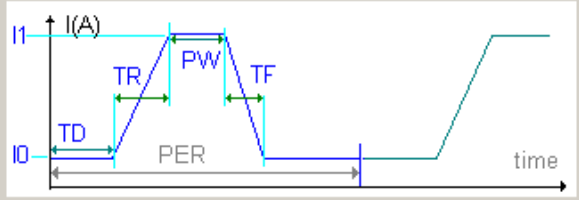
Pulse parameters

I0 (A): I1 (A):

TD (ns): TR(ns): TF(ns):

PW(ns): Period (ns):

Source frequency: 100.000 MHz



The graph shows a current pulse I(A) over time. The pulse starts at I0, rises to I1 with a rise time TR, stays at I1 for a pulse width PW, falls back to I0 with a fall time TF, and then remains at I0 for a period PER. The delay time TD is the time from the start of the pulse to the beginning of the rise time.

I. Exercises

- FFT of a square source

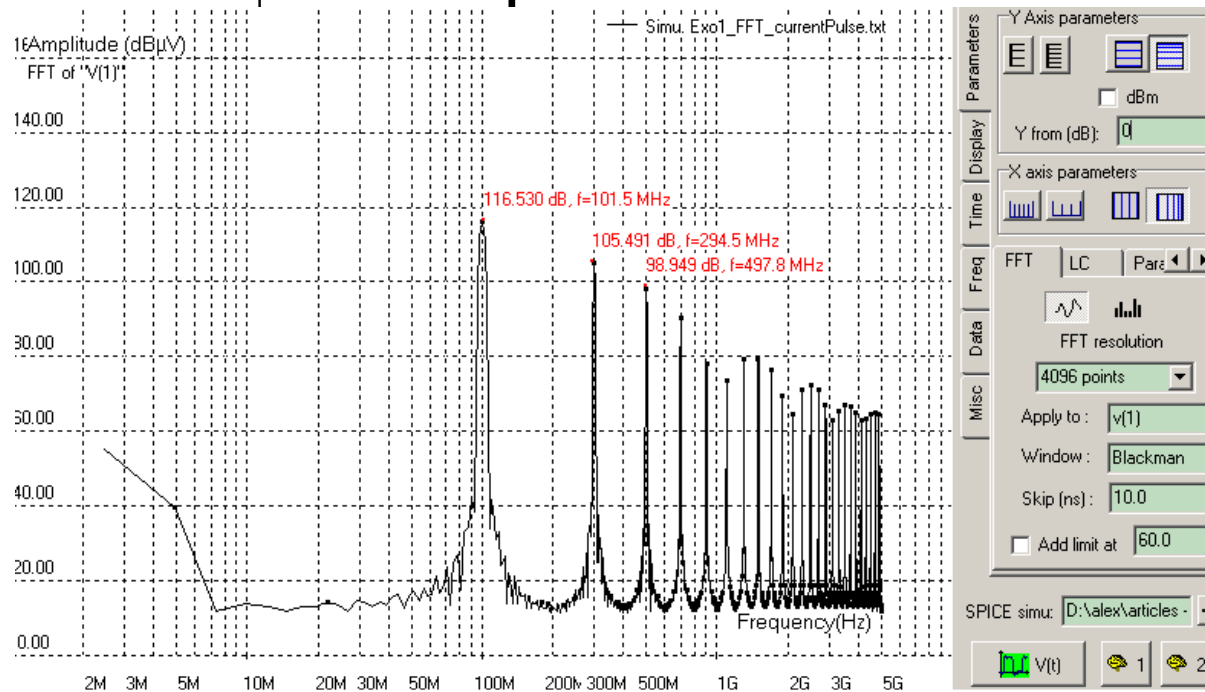
For a square signal ($T_r=0$)

$$|c_n^+| = \frac{2A\tau}{T} \left| \frac{\sin\left(n\pi\frac{\tau}{T}\right)}{n\pi\frac{\tau}{T}} \right|, n > 0$$

$$c_0 = \frac{A\tau}{T}$$

For a trapezoidal signal ($T_r=T_f$)

$$|c_n^+| = \frac{2A\tau}{T} \left| \frac{\sin\left(n\pi\frac{\tau}{T}\right)}{n\pi\frac{\tau}{T}} \right| \left| \frac{\sin\left(n\pi\frac{t_r}{T}\right)}{n\pi\frac{t_r}{T}} \right|, n > 0$$

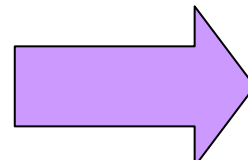
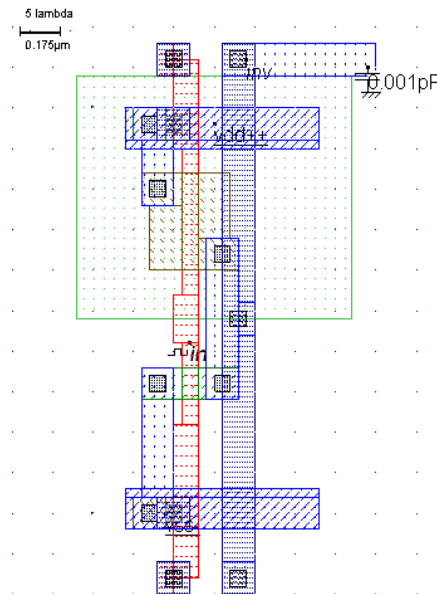
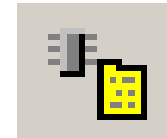


I. Exercises

- FFT of a current pulse
 - Change PW, Tr and Tf to 0.5 ns.
 - Effect on the spectrum ?

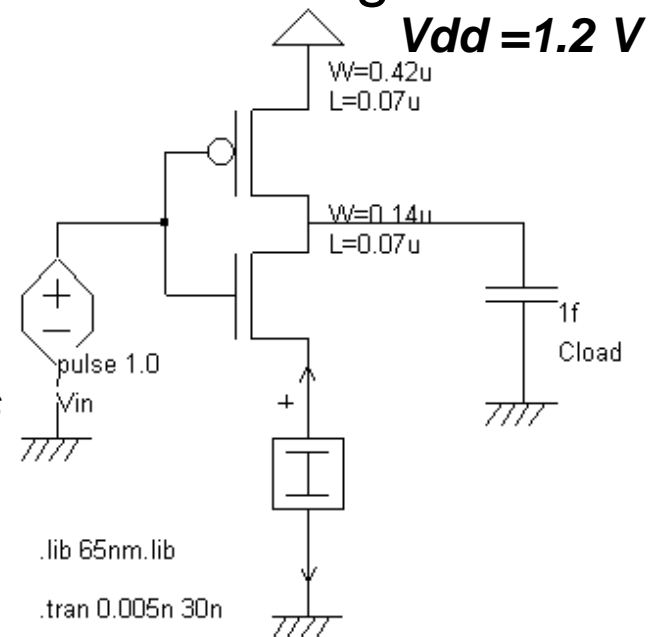
I. Exercises

- Exercise 2. Transient current estimation
 - Standard cell inverter in CMOS 65 nm (import lib\65nm.lib)
 - Typical load capacitance = 1 fF
 - Observe in time domain the current through Vss.

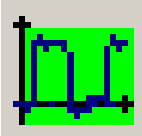



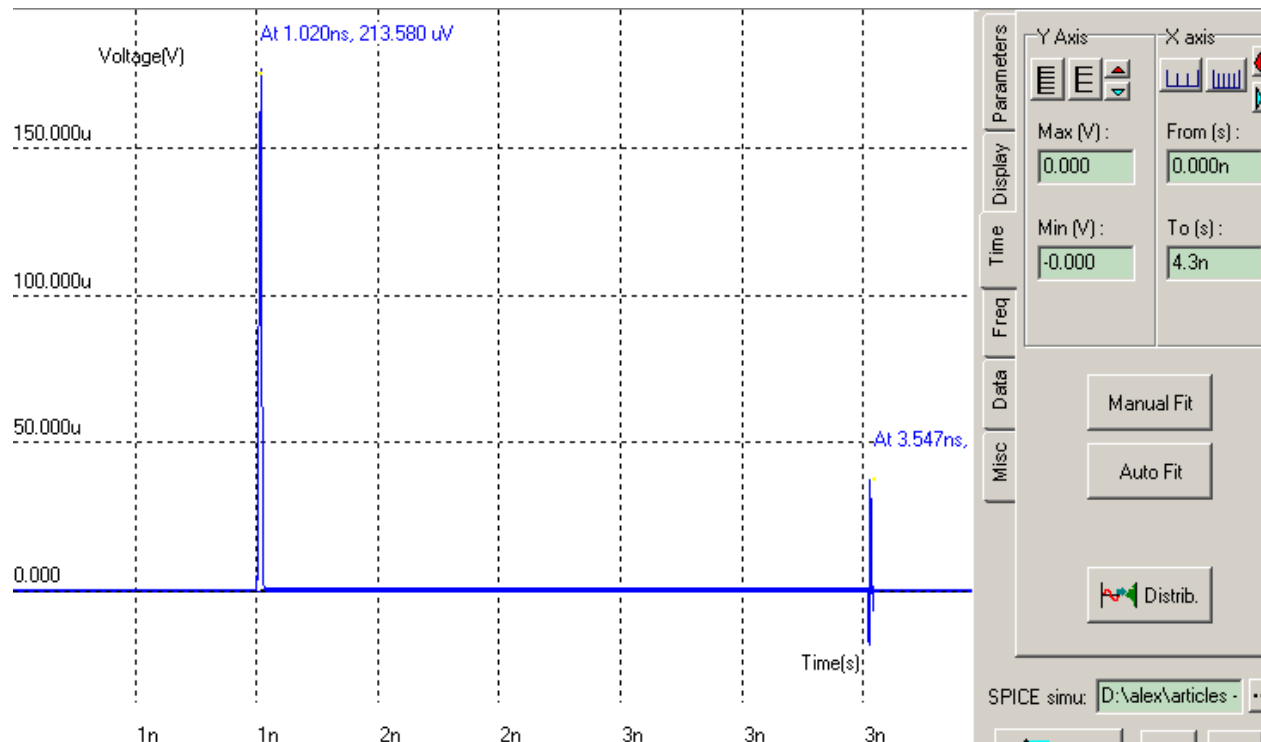
$$T_r = T_f = 20 \text{ ps}$$

$$T = 10 \text{ ns}$$



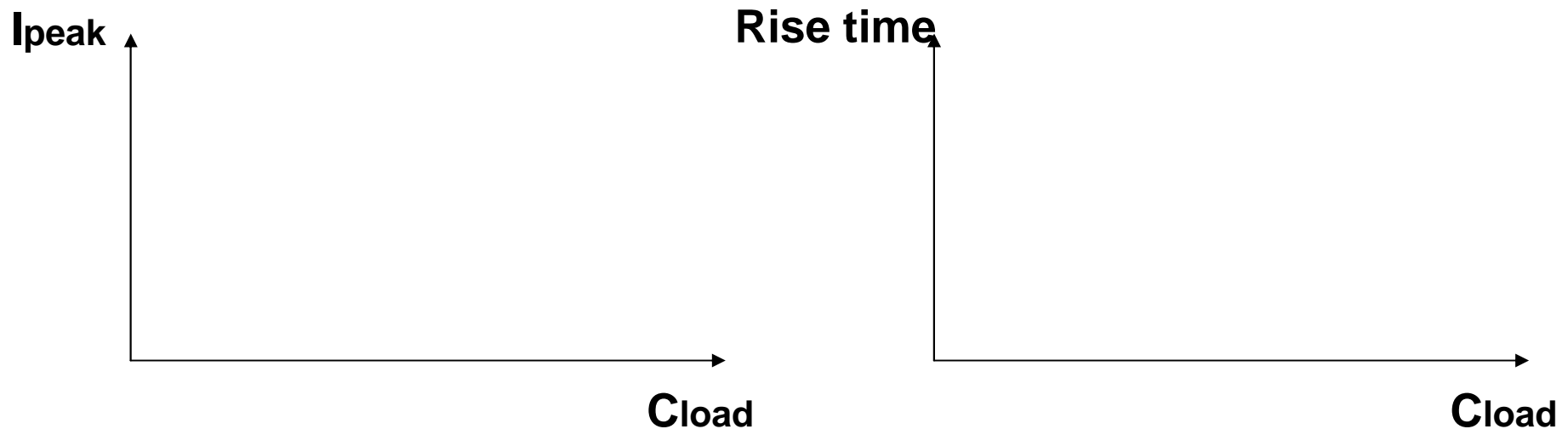
I. Exercises

- Exercise 2. Transient current estimation
 - Time domain simulation 
 - Adjust scales (Autofit and zoom on time axis) 



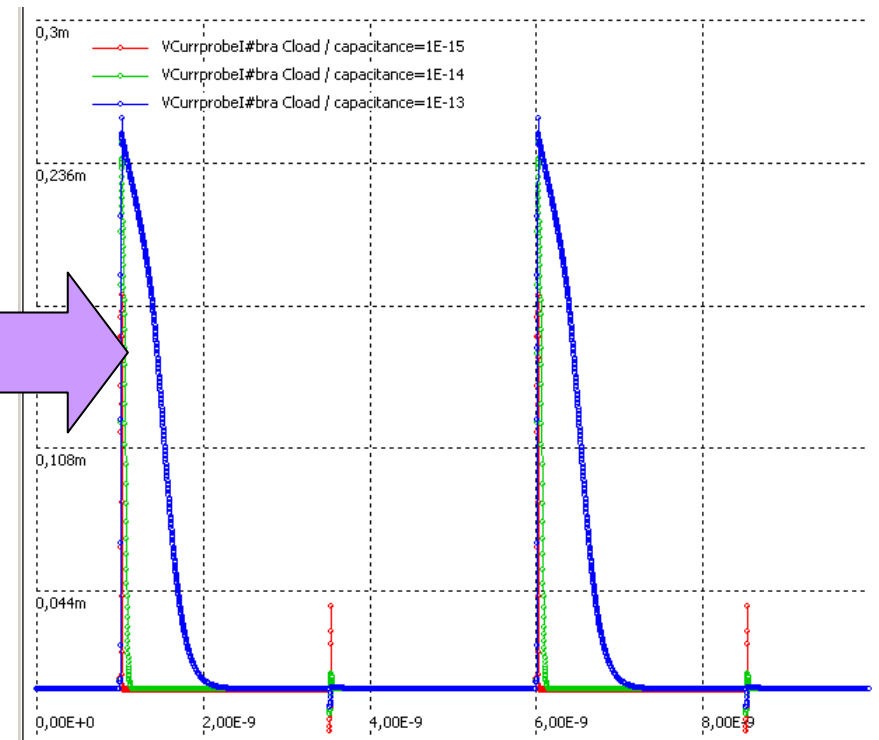
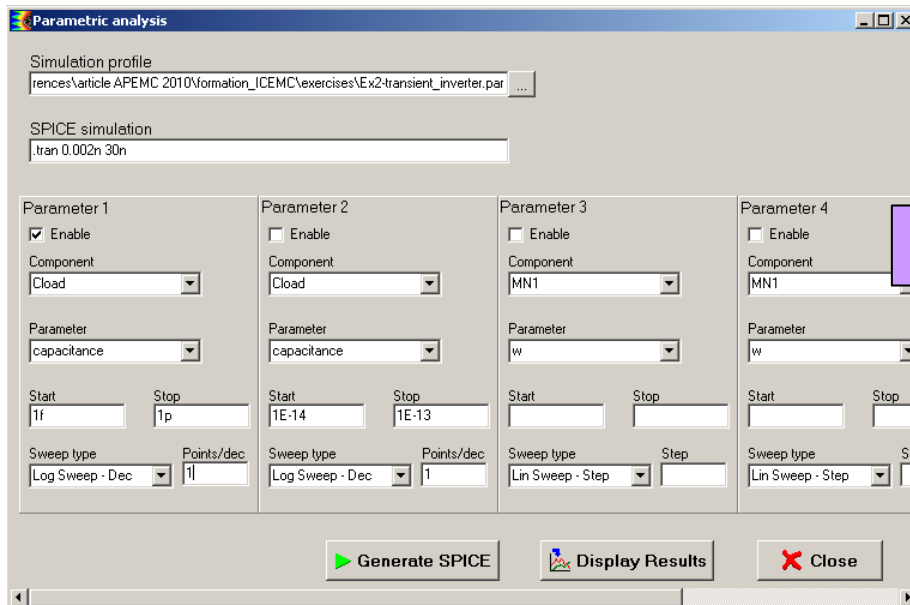
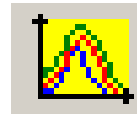
I. Exercises

- Exercise 2. Transient current estimation
 - What is the influence of the load capacitance (1 fF to 1 pF) ?



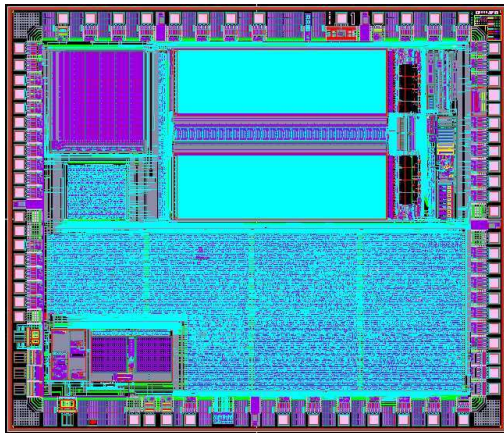
I. Exercises

- Exercise 2. Transient current estimation
 - Parametric analysis
 - Launch SPICE
 - Display results



I. Exercises

- Exercise 2. Transient current estimation
 - Consider a synchronous digital core in CMOS 65 nm formed by 100 000 gates with the following parameters:



Std cell	Number	Typical input capa (fF)	Peak current / gate (μA)
Inverter	35000	1	120
NAND2	25000	1	150
DREG	20000	2	200
NOR2	20000	1	150

- Estimate the dynamic current consumed by the circuit.

I. Basic Notions

- Exercise 2. Transient current estimation

- Raw estimation : $I_{peak} = \sum_i N_i \cdot I_{peak i}$, i : gate type

$$I_{peak} = 15 A$$

- *Does the result seem realistic ?*

I. Basic Notions

• Exercise 2. Transient current estimation

Physical Transistor
level (Spice)



Huge simulation
Limited to analog blocks

Interpolated
Transistor level



Difficult adaptation to
usual tools
Limited to 1 M devices

Gate level Activity
(Verilog)

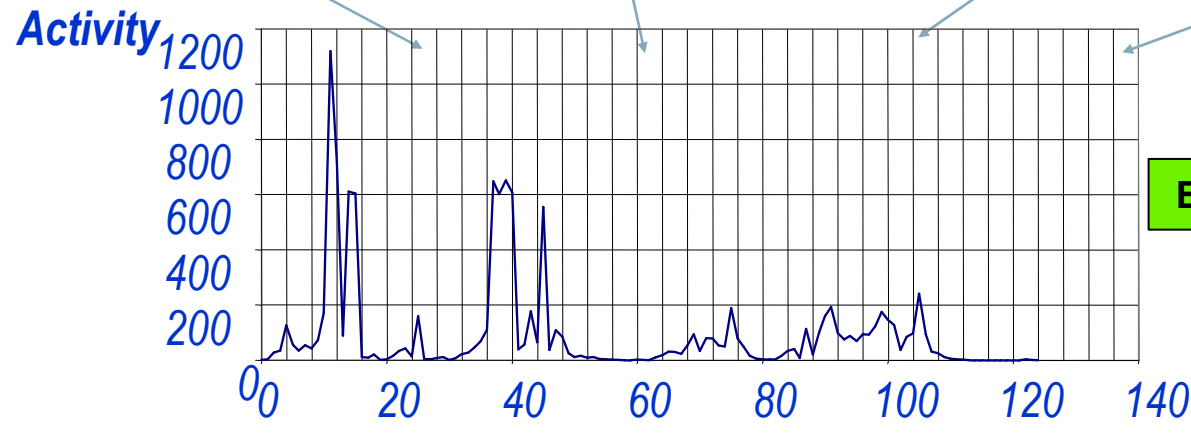


Simple, not limited
Fast & accurate

Activity estimation
from data sheet



Very simple, not limited
Immediate, not accurate



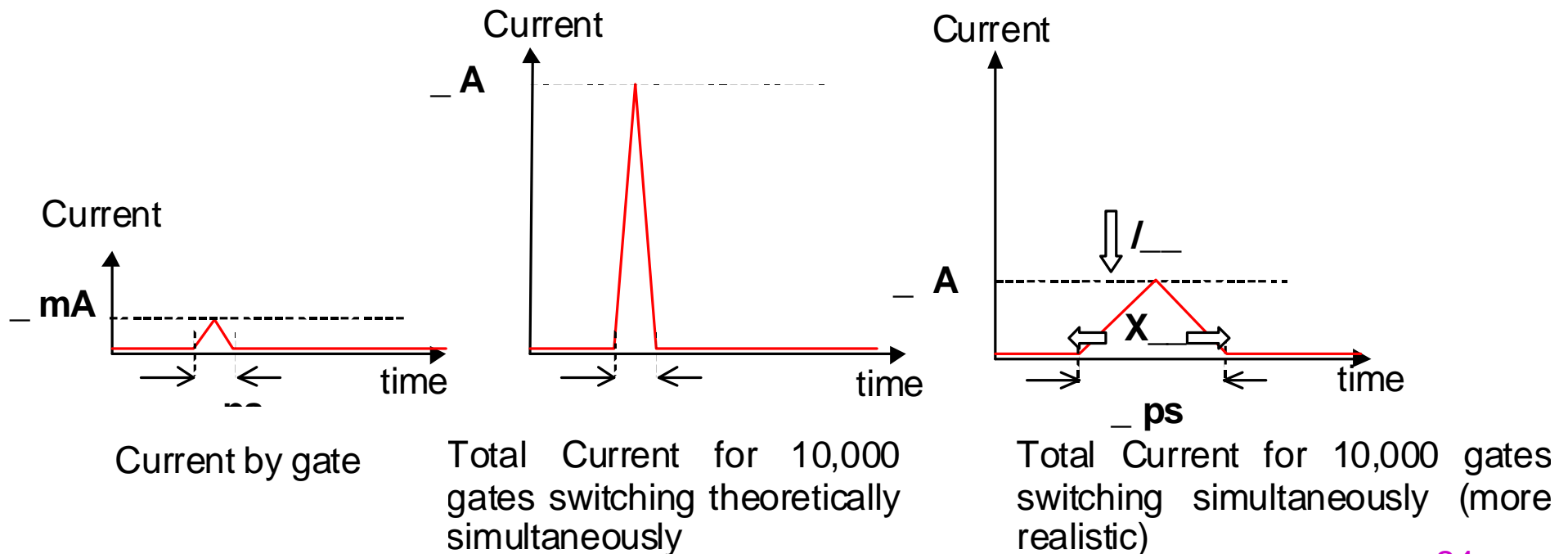
Extraction



Equivalent
Current
generator

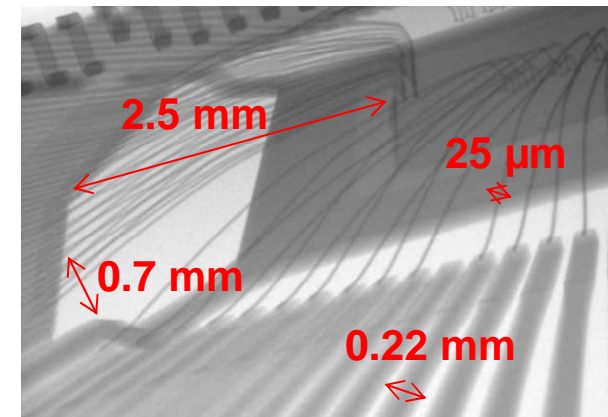
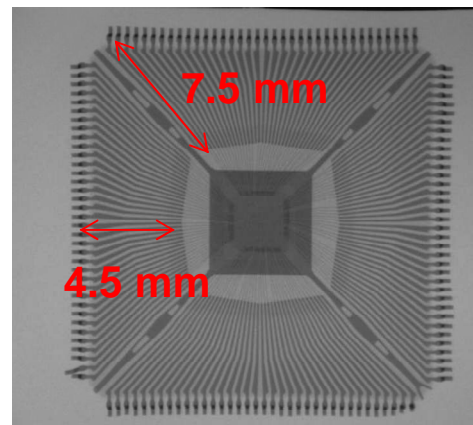
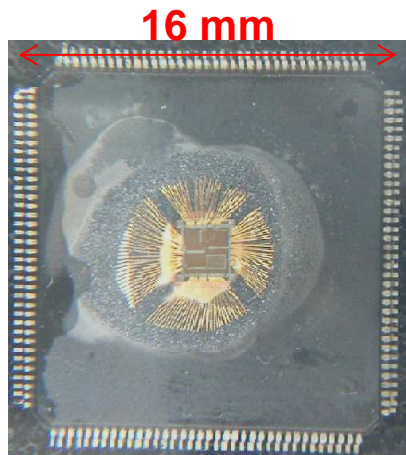
I. Exercises

- Exercise 2. Transient current estimation
 - Empirical approach : consider an activity factor of ___ % and a spread factor of ___



I. Exercises

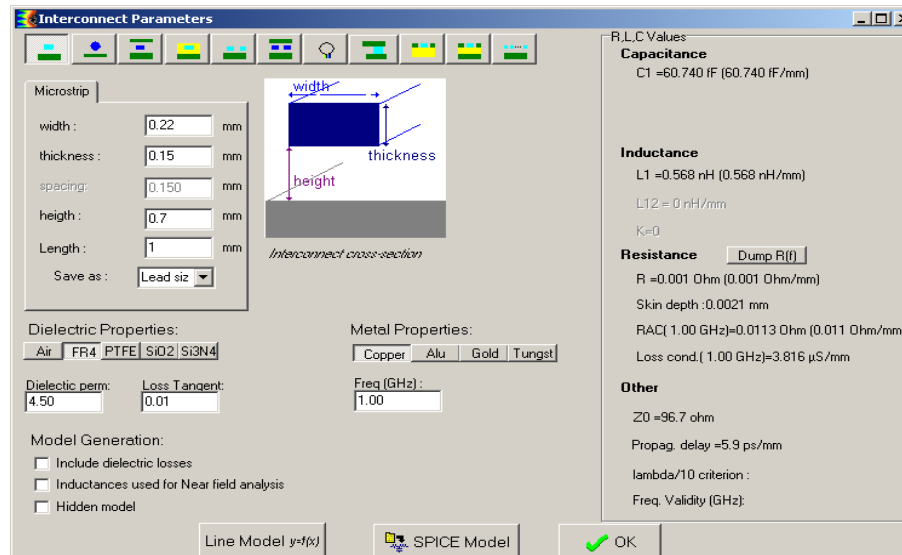
- Exercise 3. Interconnect parasitics
 - The previous core is mounted in a QFP100 package.
 - A pair of pins is dedicated to supply the core.



- Evaluate the electrical parasitic associated to the power supply pair.

I. Exercises

- Exercise 3. Interconnect parasitics
 - Use Tools/Interconnects Parameters to evaluate R, L, C associated to package pins.



$$L = \frac{\mu_o l}{2\pi} \ln \left(\frac{8h}{W} + \frac{W}{4h} \right)$$

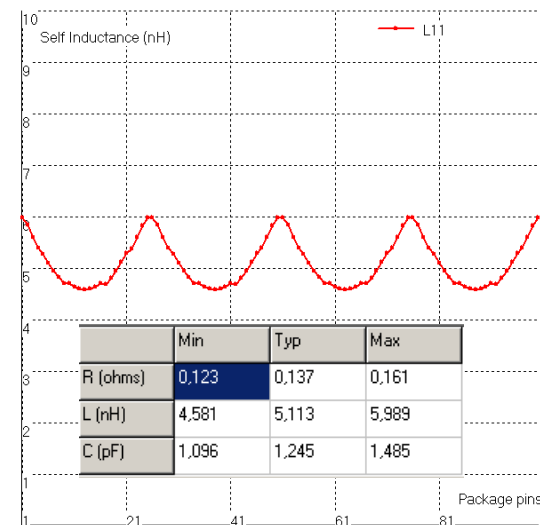
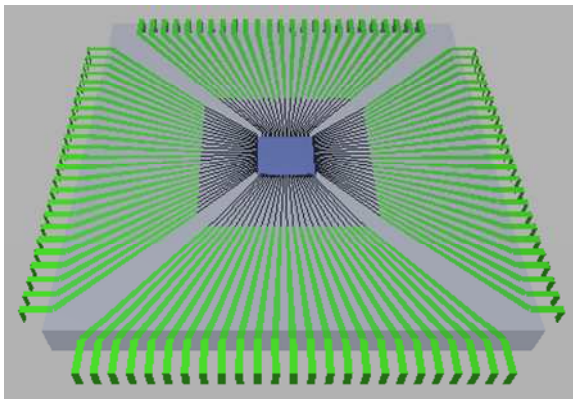
$$L = \frac{\mu_o l}{2\pi} \times \ln \left(\frac{4h}{r} \right)$$

– Empirical estimation :

- Lead : L = 0.5 nH/mm and C = 0.1 pF/mm
- Bonding : L = 1 nH/mm

I. Exercises

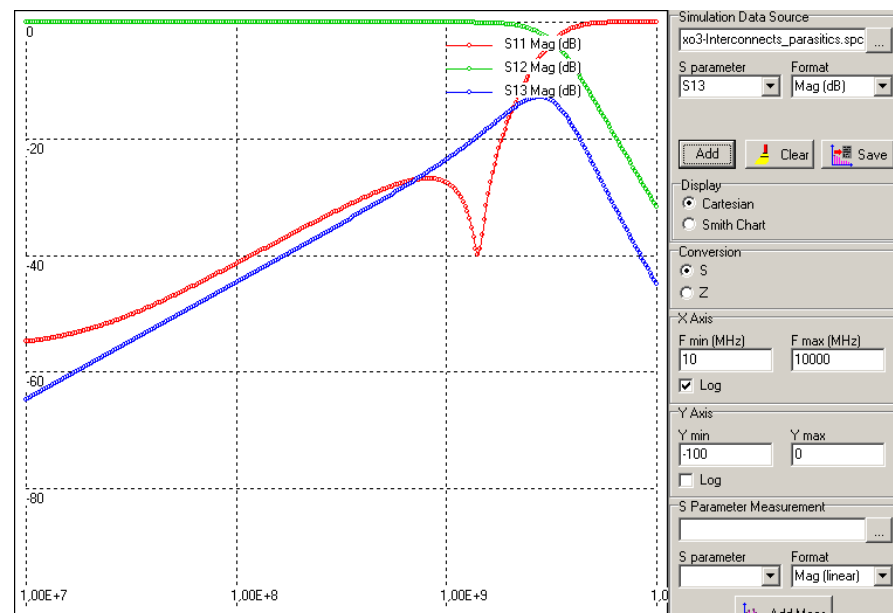
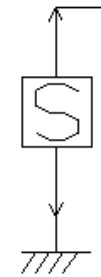
- Exercise 3. Interconnect parasitics
 - Accurate extraction of electrical interconnects based on 3D geometrical model and numerical solver.
 - Launch Tool/Advanced Package Model tool and import misc\package_model\qfp100.geo



Propose an equivalent model of the supply pair ? 27

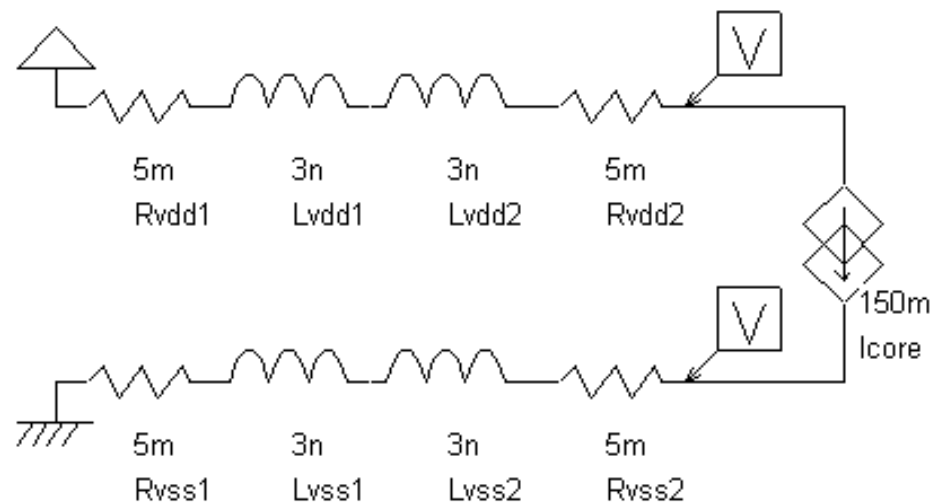
I. Exercises

- Exercise 3. Interconnect parasitics
 - Parasitic impedance of package interconnects
 - Place Ports to package access
 - Launch an .AC simulation
 - Open the S Parameter window



I. Exercises

- Exercise 4. di/dt noise
 - Estimate the voltage bounce on Vdd and Vss pins of the core defined in exercise 2 when it is mounted in a QFP100.
 - The core clock is 50 MHz.



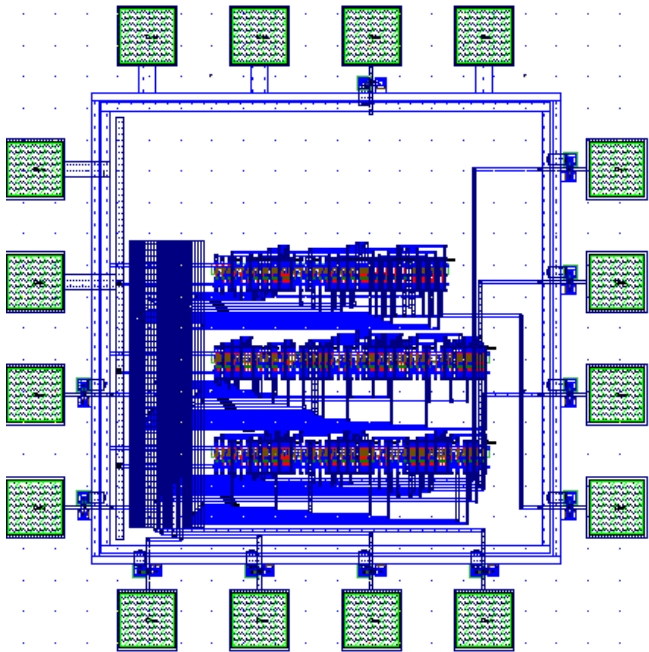
$$\Delta V = ?$$

I. Exercises

- Exercise 4. di/dt noise
 - What is the noise margin for this core ?
 - Do you consider the evaluation realistic ?

I. Exercises

- Exercise 5. On-chip decoupling

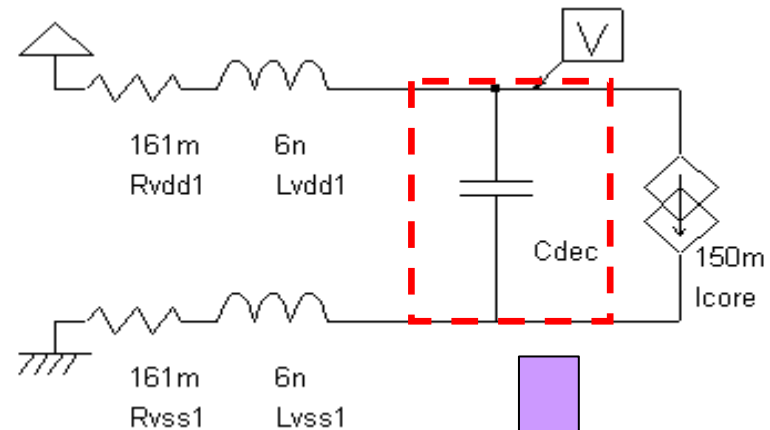


Std cell	Decoupling capacitor (fF/gate)	Size (μm^2)
Inverter	0.6	4.5
NAND2	0.9	5
DREG	5.5	25
NOR2	0.7	5

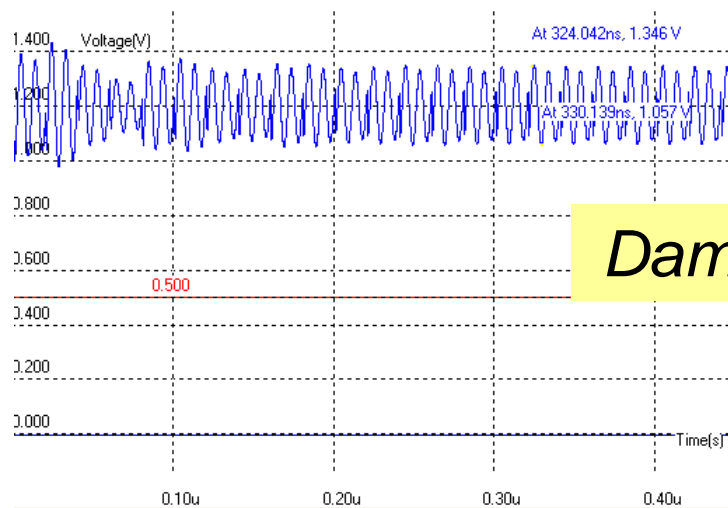
- Evaluate the intrinsic decoupling capacitor of the previous core.
- What is the effect on on-chip noise ?

I. Exercises

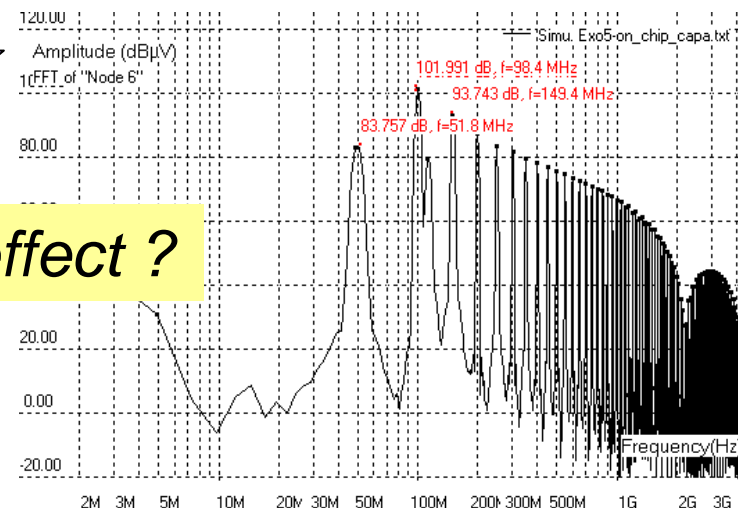
- Exercise 5. On-chip decoupling



$$C_{dec} = ?$$



Damping effect ?



I. Exercises

- Exercise 5. On-chip decoupling
 - IC power supply rails parasitics ?
 - Consider a 1 mm long and 40 μm wide Vdd or Vss line.

Metal level	Thickness	Height to substrate
M6	0.4 μm	4.5 μm
M5	0.4 μm	3.3 μm
M1	0.3 μm	0.5 μm

- Total Inductance and resistance of chip power supply rails ?

I. Exercises

- Exercise 5. On-chip decoupling

On-chip capacitor budget :

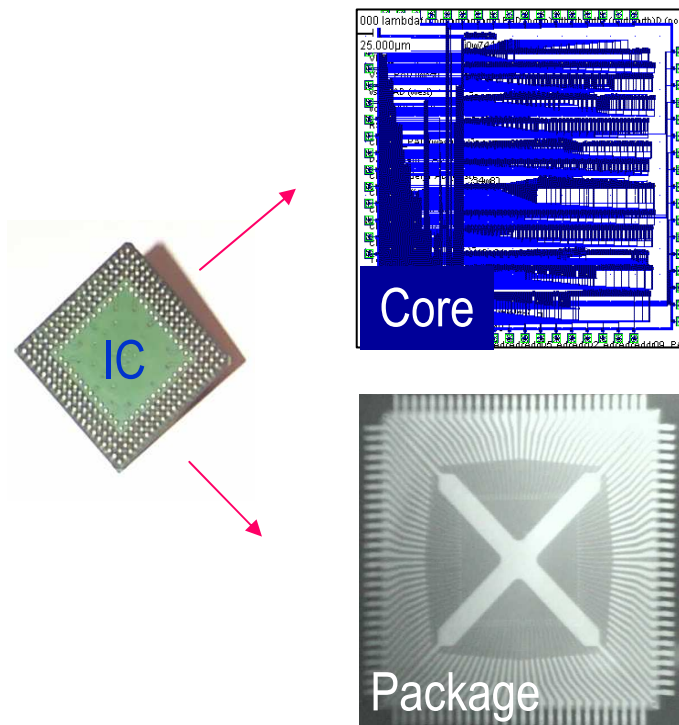
$$\Delta i = C \frac{\Delta v}{\Delta t} \Leftrightarrow C = \frac{\Delta i \times \Delta t}{\Delta v}$$

- Is the intrinsic capacitance is sufficient to reach the noise margin target ?
- How much capacitance should be added in the circuit ?

Capa. type	Capacitor density (fF/ μm^2)
Capa cell	2.2
Poly1 – Poly2	1.7
MIM	1.4

I. Exercises

- Exercise 5. Introduction to ICEM model
 - The IC model can be derived from its physical architecture, including the core and package model.



Model of the die :

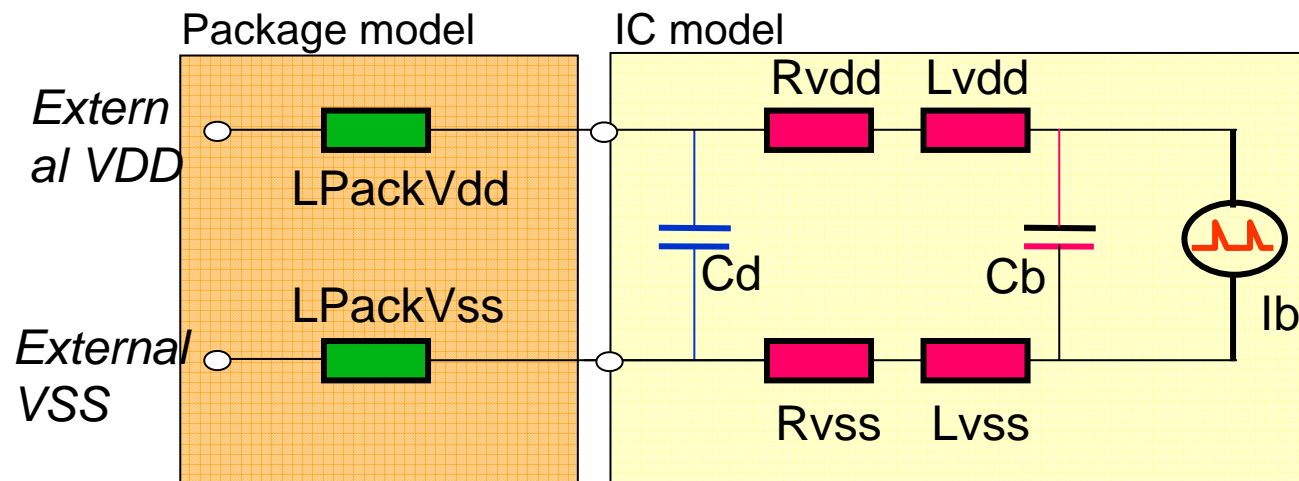
- internal activity (core)
- on-chip decoupling
- supply network
- I/O structure

Model of the package :

- R,L,C
- Transmission line

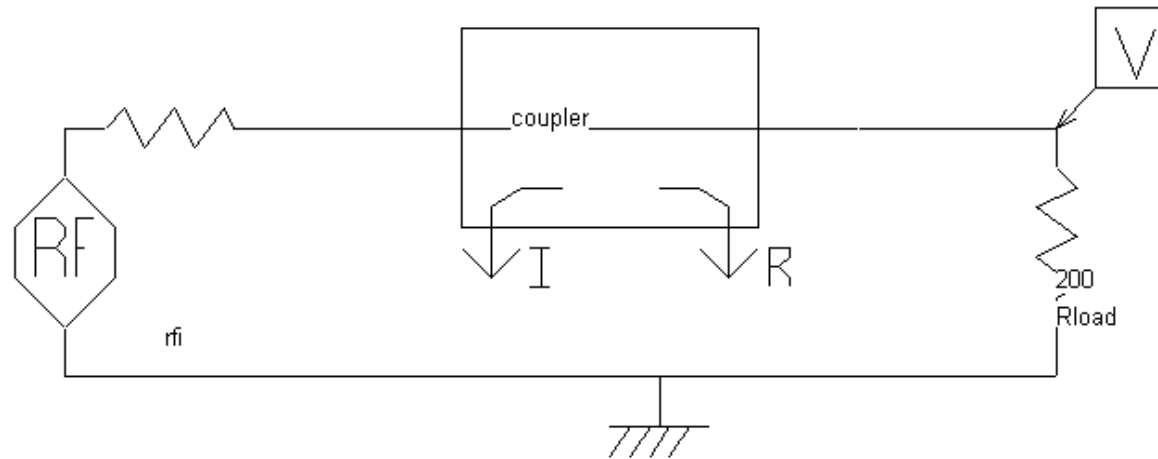
I. Exercises

- Exercise 5. Introduction to ICEM model
 - IEC 62433 – 2 : Integrated Circuit Equivalent Model
 - Equivalent model for conducted/radiated emission at IC level
 - Comment on the structure of the model.



I. Exercises

- Exercise 6. Estimation of susceptibility level
 - A RF generator produces a conducted disturbance which is injected on a $200\ \Omega$ load, though a directional coupler.




- Estimate the forward power to induce 1 V across the load over the frequency range 10 MHz – 1 GHz.

I. Exercises

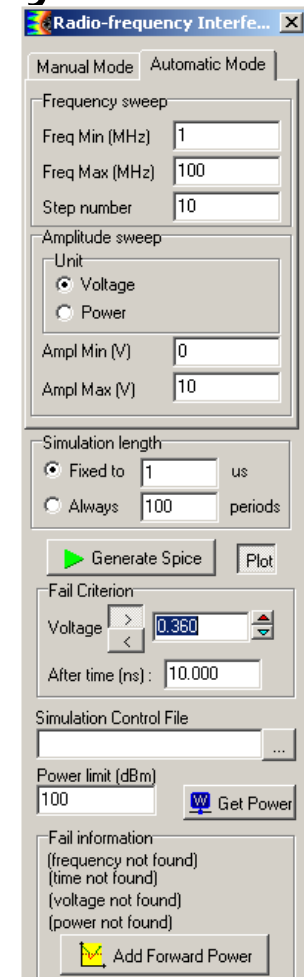
- Exercise 6. Estimation of susceptibility level

- Launch Susceptibility tool 

- Configure the RF disturbance and launch SPICE simulation

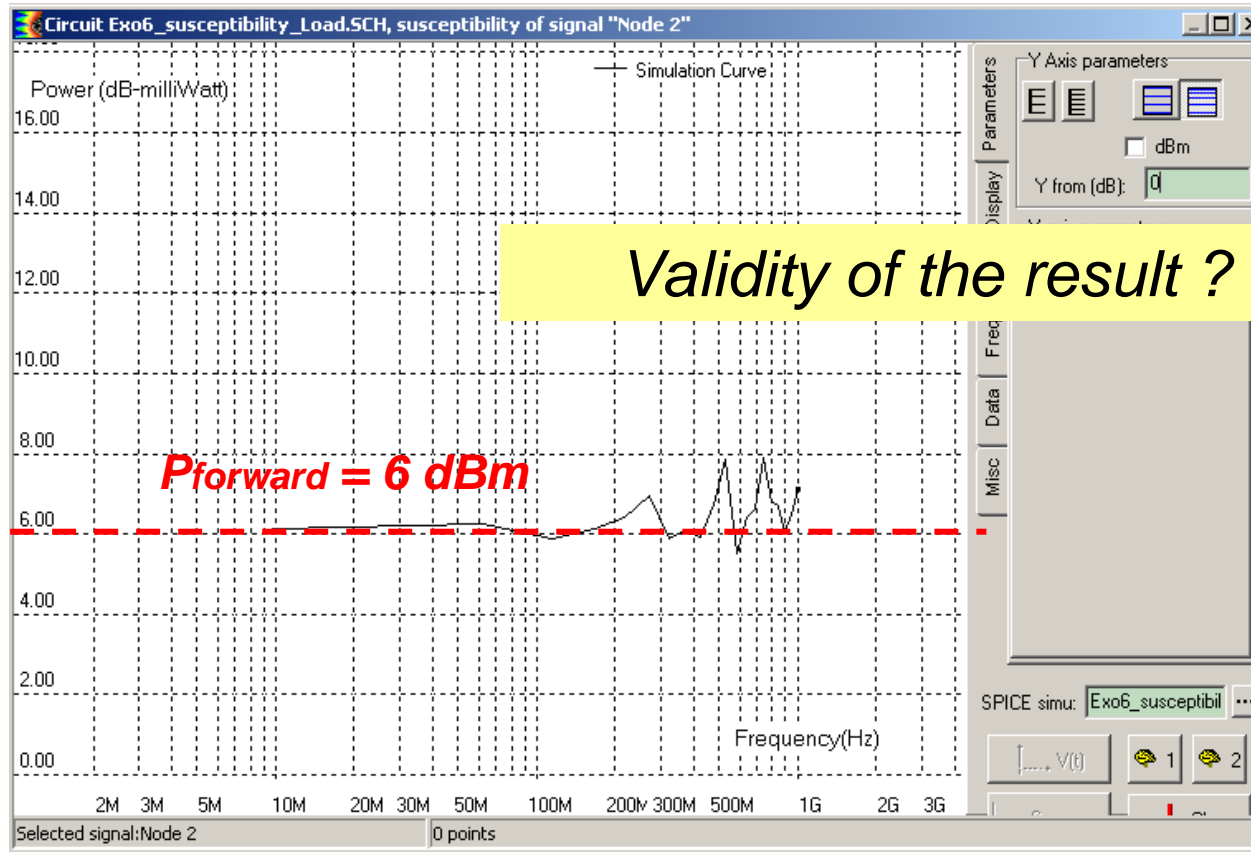
- Configure the voltage criterion and extract susceptibility threshold 

- Display the susceptibility threshold



I. Exercises

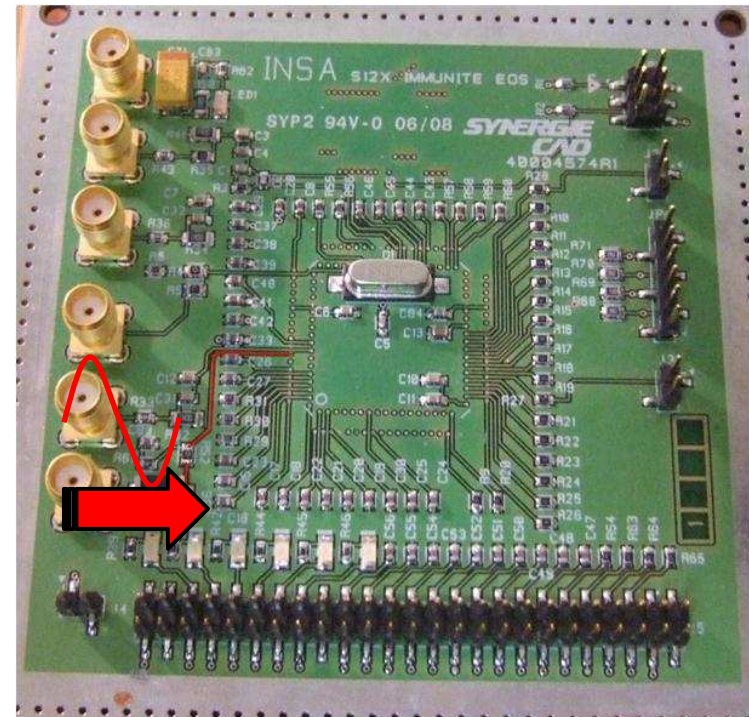
- Exercise 6. Estimation of susceptibility level



I. Exercises

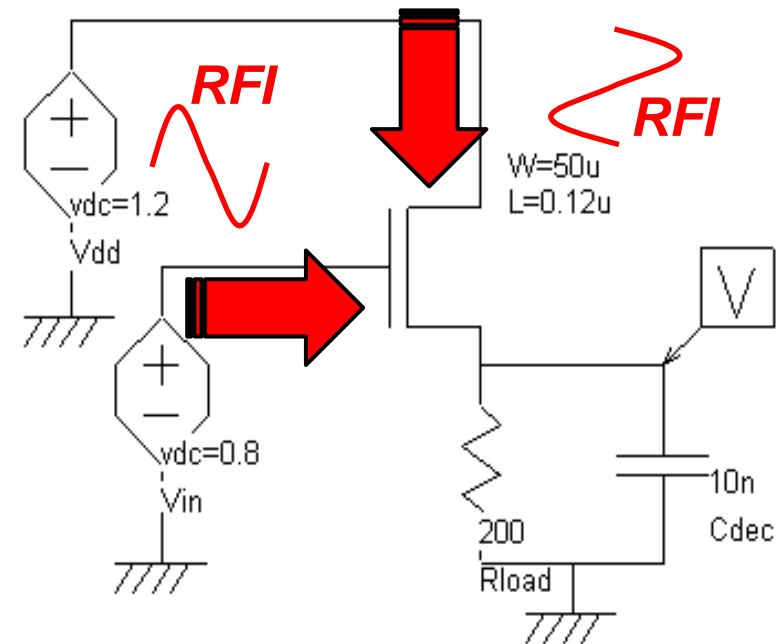
- Exercise 6. Estimation of susceptibility level

- A RF disturbance is conducted to an analog input.
- Equivalent model: serial 1 K Ω resistor and a 22 pF capacitor.
- Susceptibility criterion : input noise < 100 mV from 10 MHz to 1 GHz.



I. Exercises

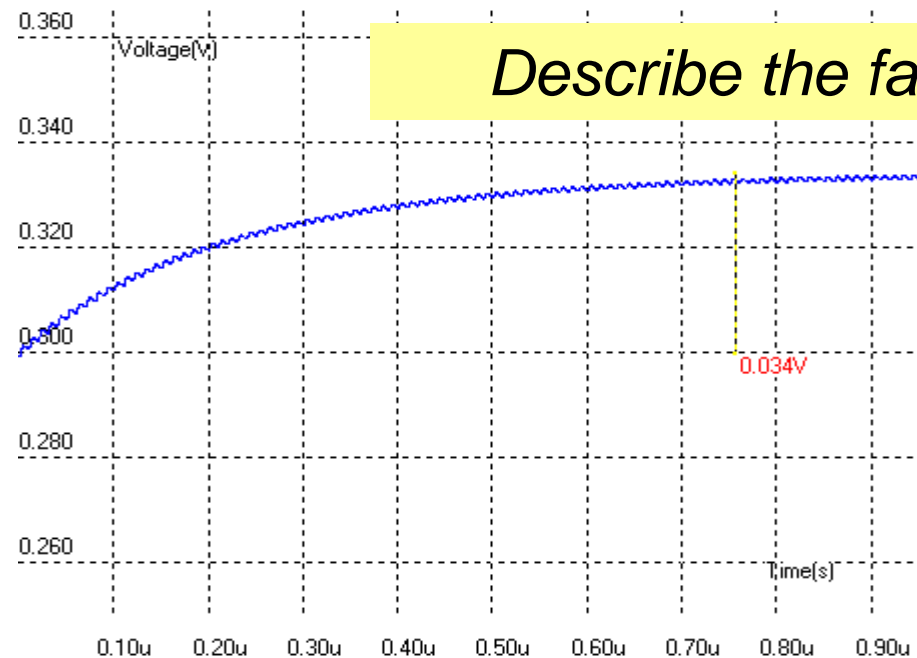
- Exercise 7. Immunity of an output buffer
 - Output buffer based on a source follower configuration.
 - The output is loaded by a 200 Ω load and a 10 nF decoupling capacitance.
 - Susceptibility of the buffer is tested with conducted injection on power supply and command input.



Susceptibility criterion ?

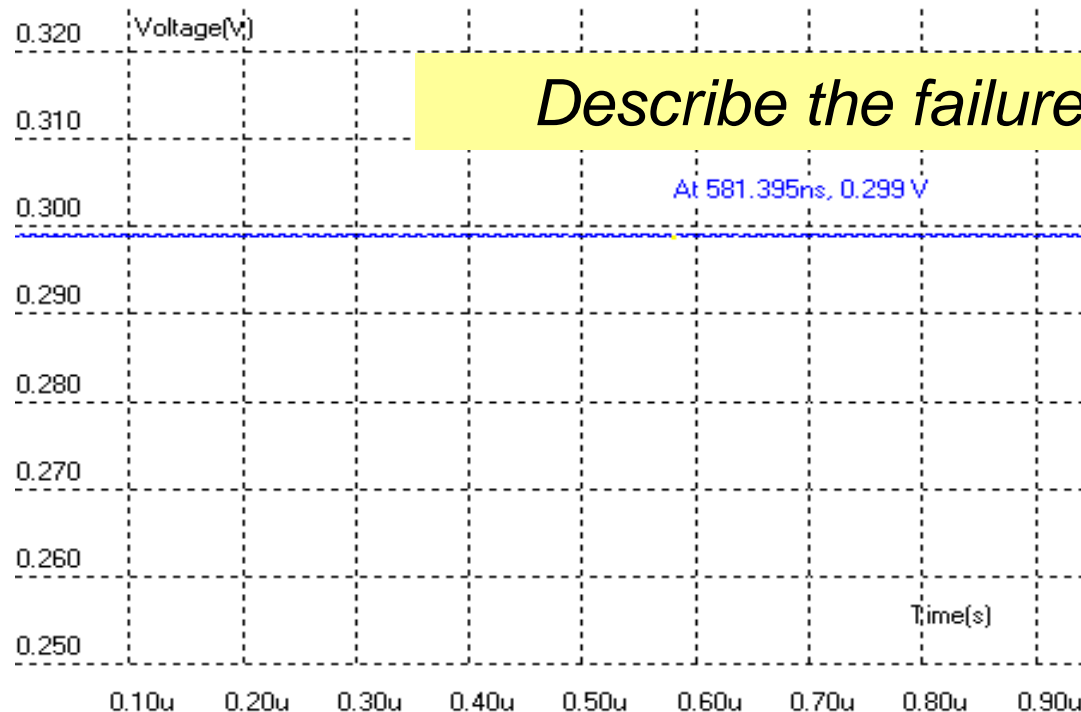
I. Exercises

- Exercise 7. Immunity of an output buffer
 - Injection on the command input
 - Add a 100 MHz RFI sinus signal on the gate node with 100 mV amplitude



I. Exercises

- Exercise 7. Immunity of an output buffer
 - Injection on the Vdd pin
 - Add a 100 MHz RFI sinus signal on the drain node with 100 mV amplitude



I. Exercises

- Exercise 7. Immunity of an output buffer
 - Failure due to rectification effect.
 - Equation of drain current based on MOS Model 1:

$$I_{ds} = \frac{\beta}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

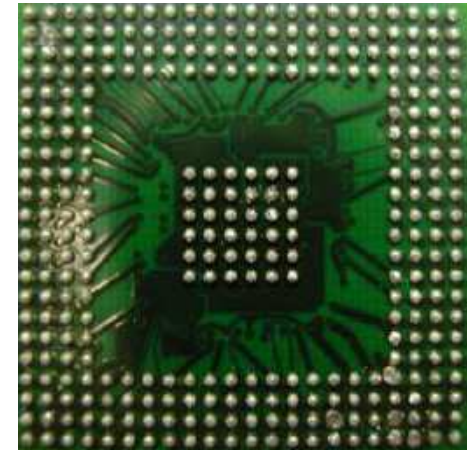
Square function → Non linear behavior

II. Advanced problems

- Problems done by group of two persons.
- Choose one problem and solve it in autonomy.
- Use the technical annexes given after problems terms.
- Proposed problems
 - 1. IC emission model construction
 - 2. Immunity model of a digital core

II. Advanced problems

- Problem 1. IC emission model construction
 - Consider the following digital circuit:
 - CMOS 65nm technology
 - 32 bits CPU, 250 K gates, surface = 3 mm², clock frequency = 25 MHz
 - The core is supplied by 4 dedicated power supply pairs
 - The IC is mounted in a 324-pin BGA package
 - The circuit is soldered on a 150×100 mm FR4 printed circuit board, with 2 internal power supply and ground planes.



II. Advanced problems

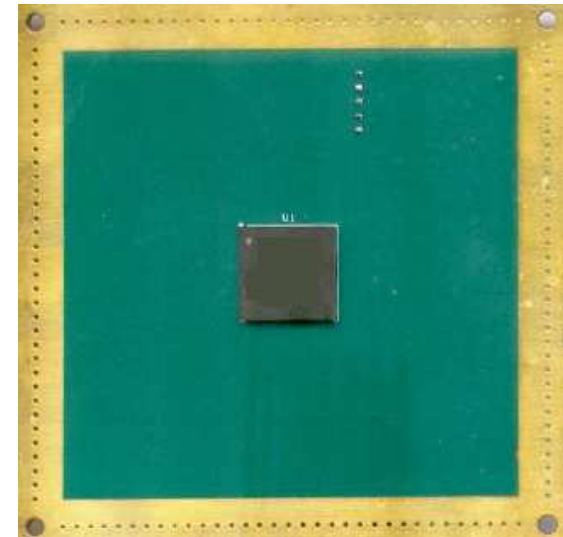
- Problem 1. IC emission model construction
 - This circuit must comply to conducted emission standard test (IEC 61967-4 – “1 Ω method “)
 - Build an equivalent ICEM model of the circuit. (*Suggestion: use Tools/ICEM model expert*)
 - Build a model of the PCB and add the 1 Ω probe for conducted emission measurement.
 - Predict the conducted emission level of the circuit using this model.
 - Add on-chip and off-chip decoupling in order to reduce the emission level under 60 dB μ V over the range 150 KHz – 1 GHz.

II. Advanced problems

- Problem 2. Immunity model of a digital core

- Consider the following digital circuit:

- CMOS 65nm technology
- 32 bits CPU, 250 K gates, surface = 3 mm²,
- The core is supplied by 4 dedicated power supply pairs
- The IC is mounted in a 324-pin BGA package
- The circuit is soldered on a 150×100 mm FR4 printed circuit board, with 2 internal power supply and ground planes.



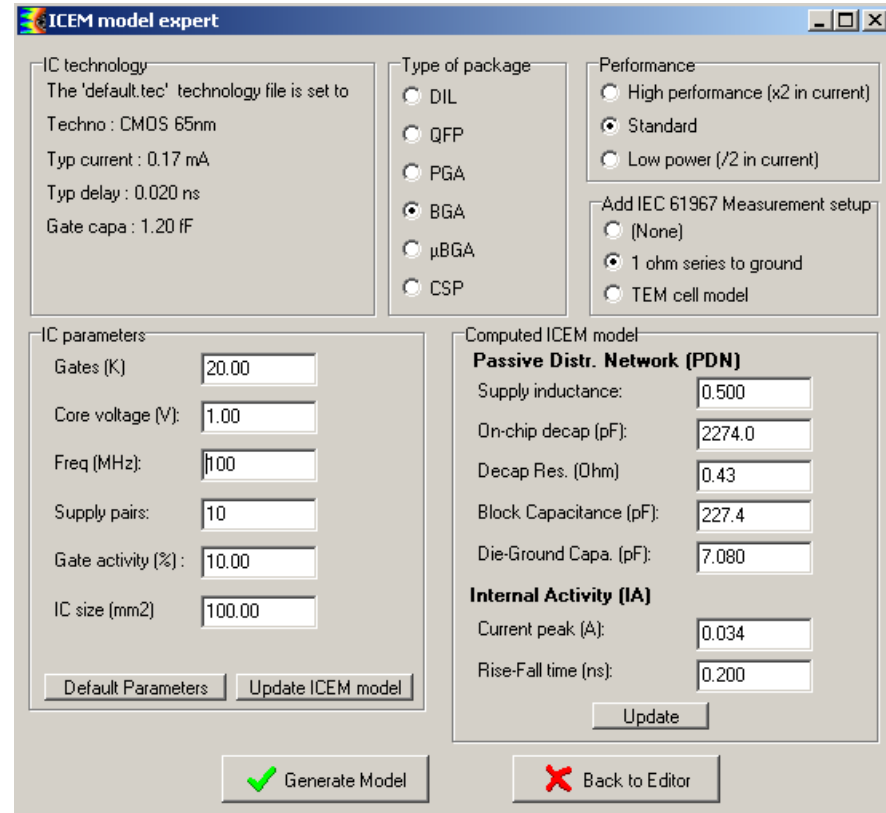
- The functionality of the core is preserved if the noise coupled on power supply is less than 0.3 V.

II. Advanced problems

- Problem 2. Immunity model of a digital core
 - This circuit must comply to conducted emission standard test IEC62132-3 Direct Power Injection (DPI) standard.
 - Test characteristics: frequency range = 1 MHz – 1 GHz, power limited to 25 dBm.
 - Build an equivalent model of the core. (Suggestion: use *Tools/ICEM model expert*)
 - Build the PCB and the injection path models.
 - Predict by simulation the susceptibility threshold of the component.
 - Compare the internal and external coupled noise.

II. Advanced problems

- Annex 1. ICEM model expert
 - Load tec file (File/Select Technology):
lib\cmos65n.tec
 - Launch Tools/ICEM Model Expert
 - Set IC technological parameters
 - Generate ICEM model



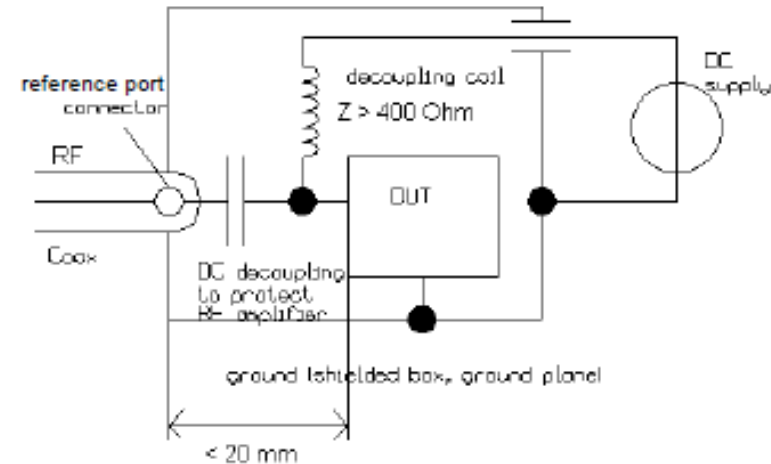
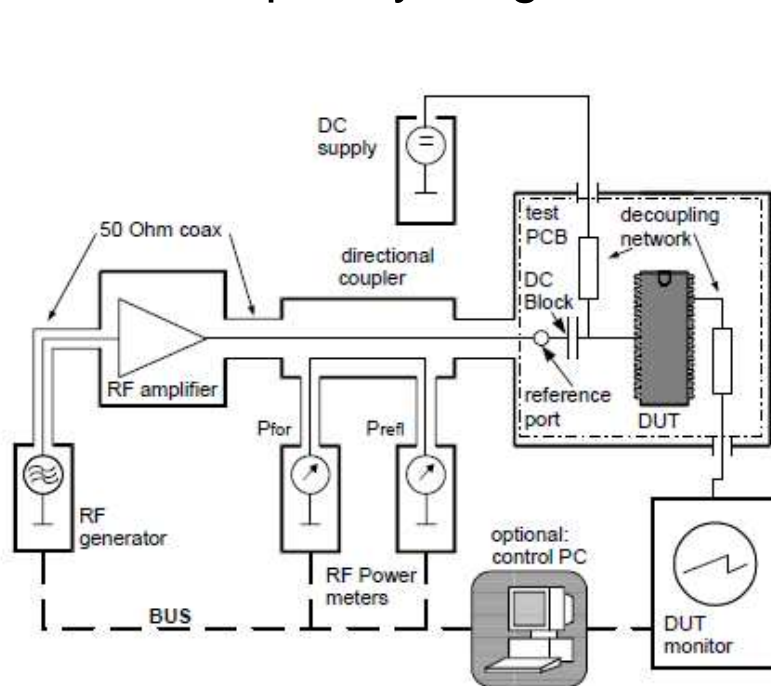
The screenshot shows the 'ICEM model expert' window with the following settings:

- IC technology:** The 'default.tec' technology file is set to Techno : CMOS 65nm, Typ current : 0.17 mA, Typ delay : 0.020 ns, Gate capa : 1.20 fF.
- Type of package:** BGA (selected).
- Performance:** Standard (selected).
- IC parameters:** Gates (K): 20.00, Core voltage (V): 1.00, Freq (MHz): 100, Supply pairs: 10, Gate activity (%): 10.00, IC size (mm²): 100.00.
- Computed ICEM model:**
 - Passive Distr. Network (PDN):** Supply inductance: 0.500, On-chip decap (pF): 2274.0, Decap Res. (Ohm): 0.43, Block Capacitance (pF): 227.4, Die-Ground Capa. (pF): 7.080.
 - Internal Activity (IA):** Current peak (A): 0.034, Rise-Fall time (ns): 0.200.

Buttons at the bottom: Default Parameters, Update ICEM model, Generate Model (with a green checkmark), and Back to Editor (with a red X).

II. Advanced problems

- Annex 3. IEC 61967-3 – DPI method
 - Scope: measurement of the susceptibility to conducted RF disturbances (RF forward power).
 - Frequency range: DC – 1 GHz



Zone	power (Watt)	protected by	example for devices
1	1 ... 5	only a small capacitor as filter	high side switches, power supply circuits
2	0.1 ... 0.5	L-,R-,C-low pass filter	signal conditioning devices, ABS sensor circuit, communication line driver
3	0.01 ... 0.05	no direct connection to the environment, decoupling by placing	Microcontroller, memories

From IEC 62132-3 – “Direct RF Power Injection Method”, IEC standard

II. Advanced problems

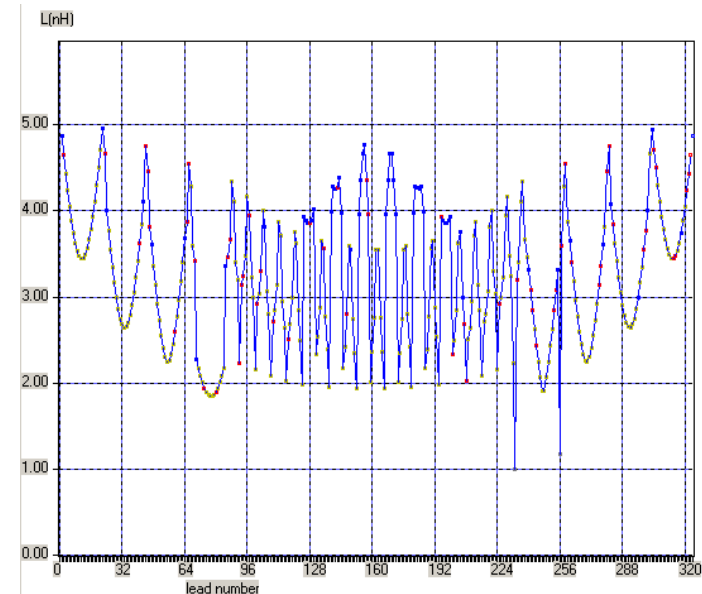
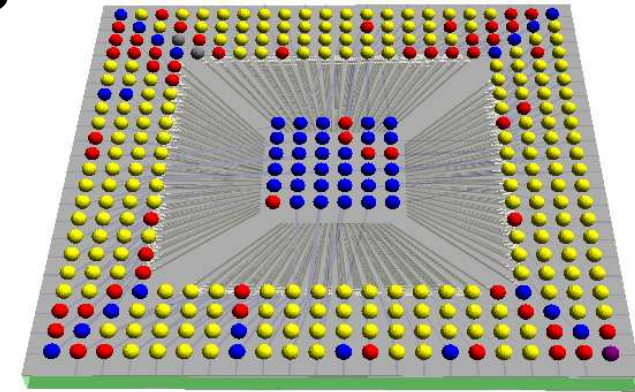
- Annex 4. BGA 324 package

- Dimensions:

- Package width: 23 mm
- Pitch: 1 mm
- Ball diameter: 0.3 mm
- IC height: 1 mm

- Typical electrical parameters:

L typical	3.3 nH
R typical	100 mΩ
C typical	0.8 pF

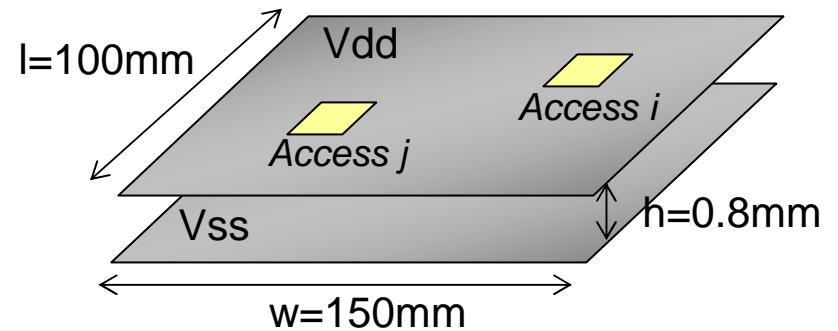


II. Advanced problems

- Annex 5. PCB power planes

- Vdd/Vss power planes form a resonant cavity.

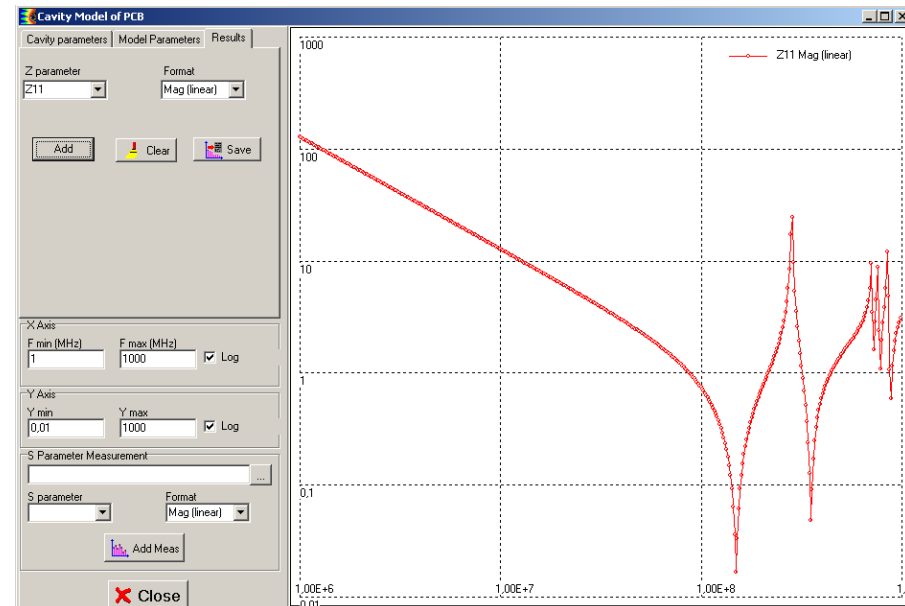
$$Z_{ij}(\omega) = \sum_i \sum_j \frac{j\omega\mu_0 h N_{mni} N_{mnj}}{w.l(k_{mn}^2 - k^2)}$$



- Extract Impedance profile with Tools/Cavity Model
- Extract an equivalent electrical model:

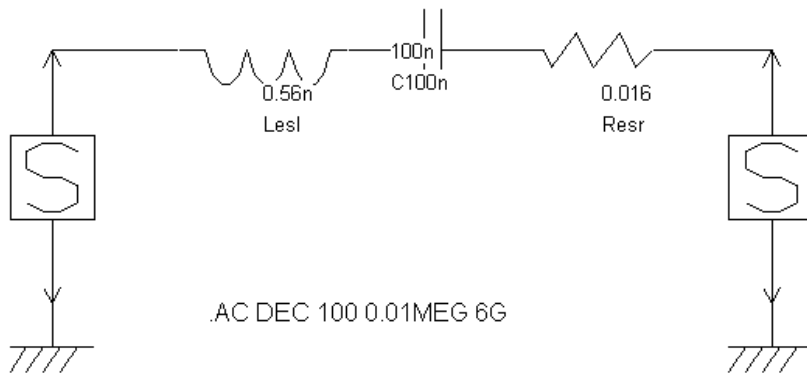
$$C = \frac{\epsilon_0 \epsilon_r w l}{h}$$

$$L = \mu_0 h$$



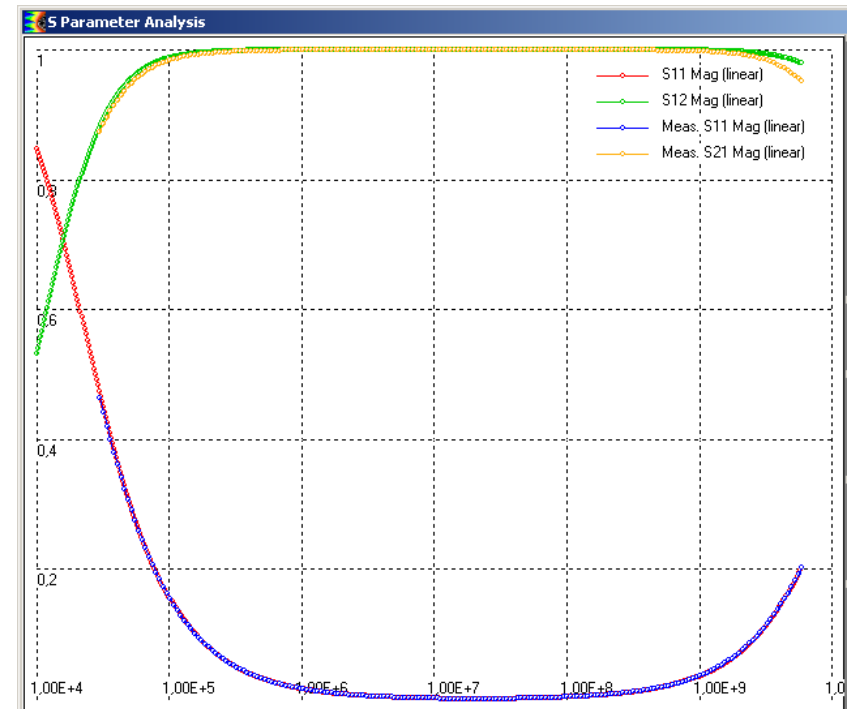
II. Advanced problems

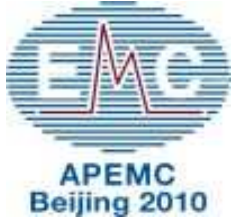
- Annex 6. Passive model
 - Import Touchtone file and schematic model of capacitance and inductance in EMC_lib\passive



Murata GCM188R72A102KA37

Ceramic 100nF Capacitor from Murata (0603, X7R 16 V, Automotive applications)





Thank you for your attention