Simulation of the Temperature Influence in IC-EMC

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Abstract: We investigate in this application note the performance variation with temperature of MOS devices and propose a temperature-linear model for capacitance.

Keywords: MOS, temperature, capacitance, non-linear model

Files for this case study may be found in the directory "case_study/temperature"

1 Introduction

The integrated circuit performances are strongly dependent on temperature. The main impact of temperature on MOS devices is the current drive (fig.1) which decreases significantly with temperature, leading to slower switching performances. We investigate in this application note the performance variation with temperature and analyse its impact on EMC performances of ICs.

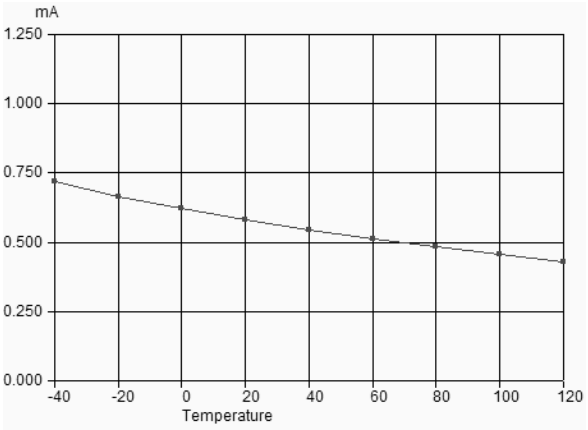


Figure 1: the Ion current decreases with temperature [1] (MOS W=10µm, L=0.12µm)

2 Temperature Modeling in MOS devices

Three main parameters are concerned by the sensitivity to temperature [1]: the threshold voltage `VTO`, the mobility `U0` and the leakage current. Both `VTO` and `U0` decrease when the temperature increases. The physical background is the degradation of the mobility of electrons and holes when the temperature increases, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers.

The modeling of the temperature effect in BSIM models [2] is as follows. `TNOM` is fixed to 300°K, equivalent to 27°C. `UTE` is negative, around -1.8, while `KT1` is around -0.06.

$$U0 = U0_{(T=27)}\left(\frac{T+273}{TNOM}\right)^{UTE} \quad \text{(Eq. 1)}$$

$$VT = VT0_{(T=27)} + KT1\left(\frac{T+273}{TNOM} - 1\right) \quad \text{(Eq. 2)}$$

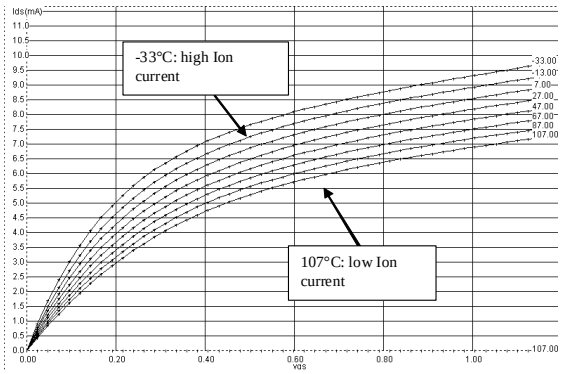


Figure 2 : The effect of temperature on the peak Ids current, showing a degradation of current with rising temperature (MOS W=10µm, L=0.12µm)

A higher temperature leads to a reduced mobility, as UTE is negative. Consequently, at a higher temperature, the current *Ids* is lowered. This trend is clearly illustrated in figure 2. The reduction of the maximum current is 40% between -30℃ and 100℃.

Meanwhile, in an opposite trend, the threshold voltage is decreased, as KT1 is negative (Figure 3). Therefore, there exists a remarkable operating point where the *Ids* current is almost constant and independent of temperature variation.

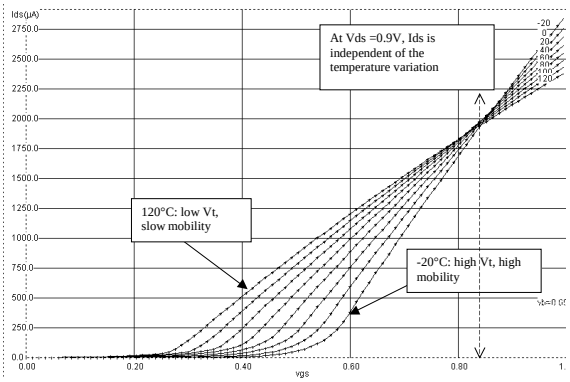


Figure 3: The effect of temperature on the Ids current, showing a zero temperature coefficient (ZTC) operating point (MOS W=10µm, L=0.12µm)

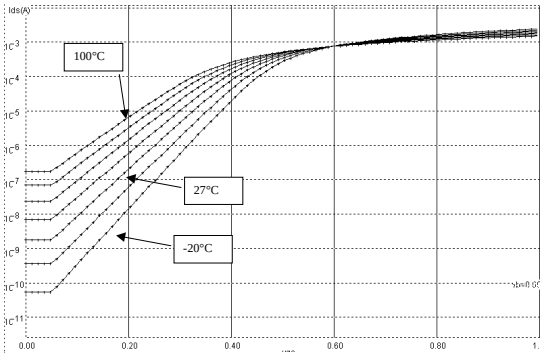


Figure 4: The effect of temperature on the MOS characteristics in sub-threshold mode (Vg<Vt)

In 0.12µm CMOS, the *Vds* voltage with zero temperature coefficient (ZTC) is around 0.9V, as shown in figure 3.

In the sub-threshold region (VG less that VTO), the impact of temperature is extremely important, as demonstrated in figure 4. At low temperature the current *Ids* decreased rapidly down to 10nA, corresponding to a small off leakage current. In contrast, at high temperature, not only the threshold voltage is reduced but the sub-threshold slope is flattened, which means an exponential increase of the *Ioff* leakage current (figure 4).

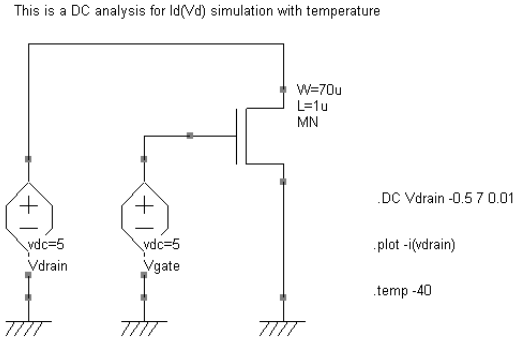


Figure 5: Study of the temperature influence on MOS characteristics (nmos_dc_iv_temp.sch)

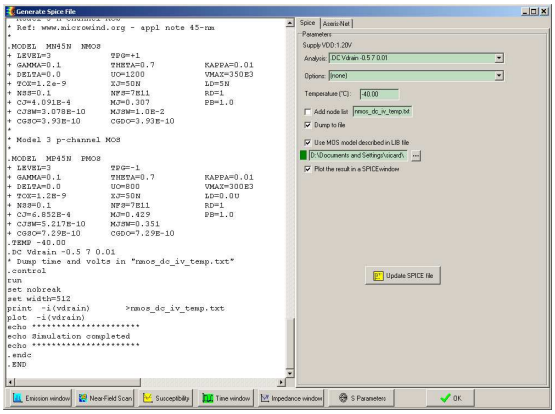
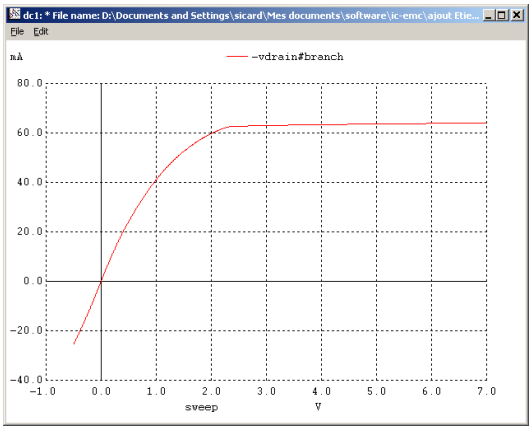


Figure 6: The temperature may be changed in the "Temperature (°C)" control situated on the right side of the Spice window (nmos_dc_iv_temp.sch)

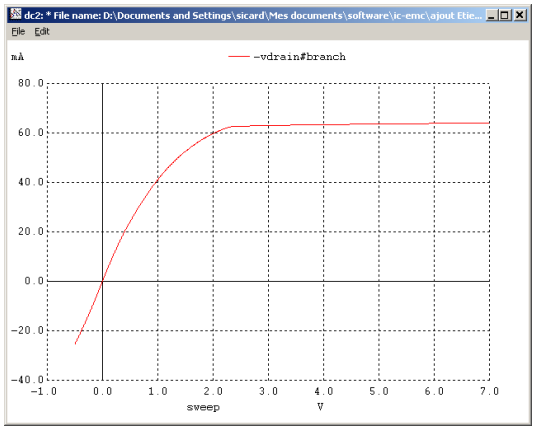
3 Temperature Simulation in IC-EMC

3.1 MOS devices

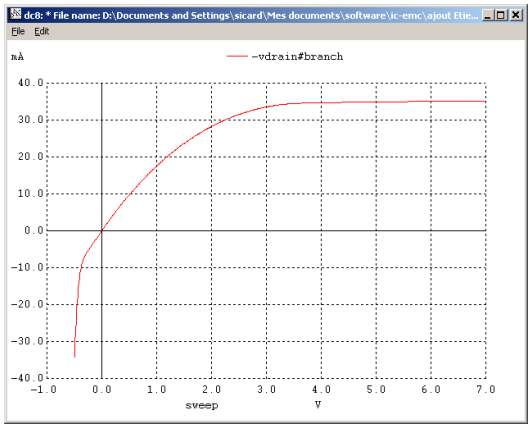
In IC-EMC, the temperature may be altered by a specific keyword ".temp <value>" directly in the schematic diagram (Fig. 5), or in the SPICE control window "Temperature (°C):" (Fig. 6). The result is the addition of a control line in the SPICE file ".temp -40.0". We change this parameter to 27 and 125 to investigate the Ion performances of the nMOS device (Fig. 7).



(a) T=-40°C



(b) T=27°C



(c) T=125°C

Figure 7: The temperature effect on static Id/Vg MOS characteristics (nmos_dc_iv_temp.sch)

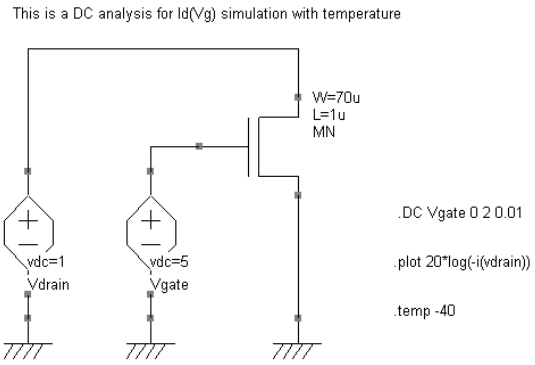
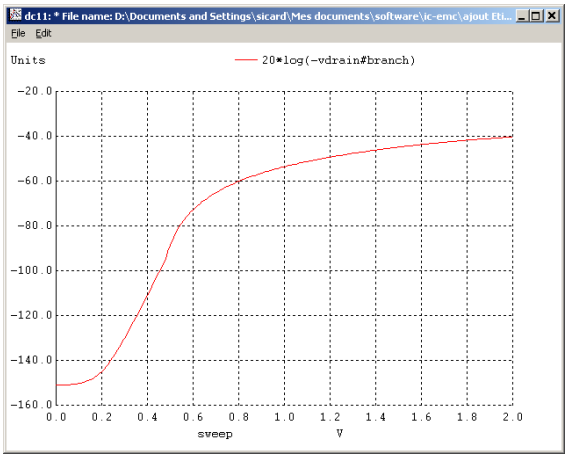
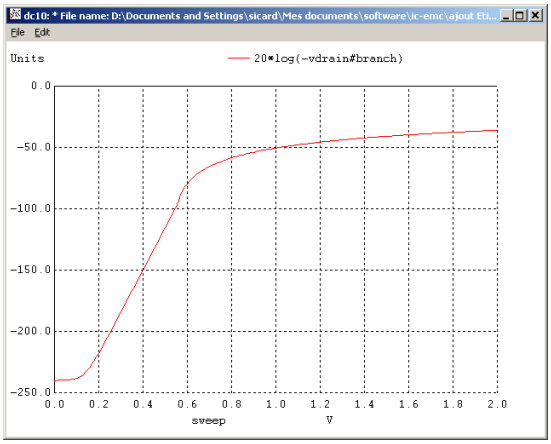


Figure 8: Setup for subthreshold simulation (nmos_dc_ioff_temp.sch)



(a) T=125°C



(b) T=-40°C

Figure 9: Simulation of the subthreshold performances for 125°C and -40°C (nmos_dc_ioff_temp.sch)

The subthreshold slope may be simulated using a control on the gate voltage, for a given Vds voltage (usually low, around 1V). The schematic diagram used for this simulation is shown in Fig. 8. Notice the request for plotting the current in dBA (0 dBA= 1A, -60 dBA = 1 mA, -120 dB = 1 µA). Fig. 9 shows a very important increase of Ioff at high temperature, as expected.

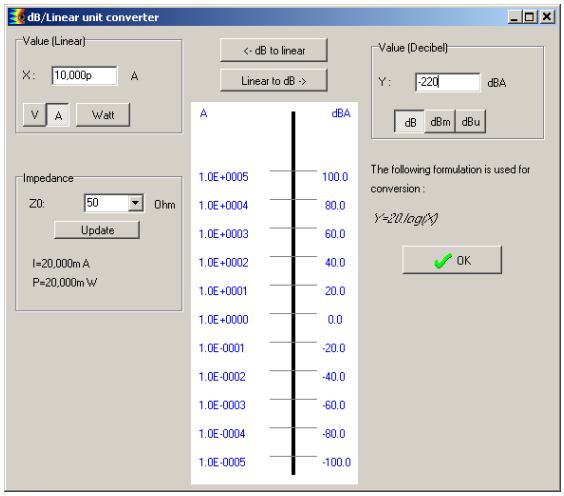


Figure 10: Using the dB/Linear Unit converter to convert dBA into A

The tool "dB/Linear Unit converter" is useful to convert the dBA scale (Y axis of Fig. 9) into A. As displayed in Fig. 10, -220 dBA corresponds to 10 pA.

3.2 Capacitance

Not only MOS devices such as the ones found in the core and in the I/Os may be temperature dependent. The decoupling capacitance usually included in the IC model is also dependent on temperature.

name	parameter	units	default	example
TNOM	nominal temperature	°C	27	50
TC1	first order temperature coefficient	Ω/°C	0.0	-0.001
TC2	second order temperature coefficient.	$\Omega/°C^2$	0.0	-0.0001

Table 1: capacitance model parameters taking into account the temperature

The usual way to handle the capacitance variation is to declare a model as follows:

```
CXXXXXXX N1 N2 <VALUE> <MODEL
NAME>
```

Example:

```
CD 3 7 1n CMODEL
.MODEL CMODEL CAP(TC1=-0.001)
```

TNOM is used to override the circuit-wide value given on the .OPTIONS control line where the parameters of this model have been measured at a different temperature. After the nominal capacitance is calculated above, it is adjusted for temperature and voltage nonlinearity by the formula, where C_0 is the capacitance value given in the field <VALUE>.

$$C_{eff} = C_0\left(1+TC_1\left(T-T_{nom}\right)+TC_2\left(T-T_{nom}\right)^2\right)$$

In IC-EMC, each capacitance may be declared as temperature dependent, trough a specific tick as shown in figure 11.

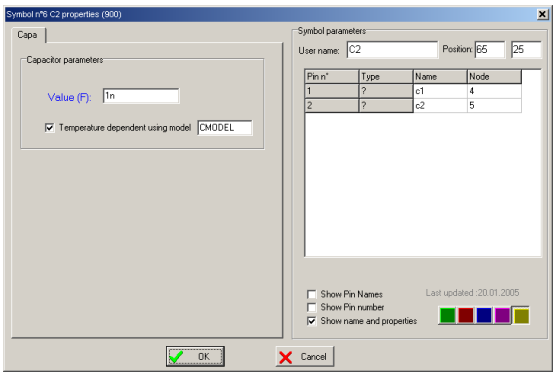


Figure 11: declaring the capacitance as temperature dependent (capa_var_temp.sch)

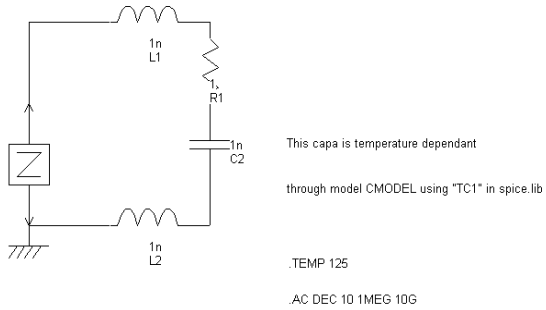


Figure 12: An example of impedance simulation versus frequency to investigate the temperature influence (capa_var_temp.sch)

The parameters of the model „CMODEL“ may be adjusted in the SPICE library „spice.lib“ that can includes a specific model description for the capacitance.

An example of temperature influence investigation is proposed in the figure 13, corresponding to the frequency domain analysis of the passive network impedance Z(f). On the schematic diagram, we place two inductances L1 and L2, as well as a capacitance C2. By a double click in the capacitance symbol and asserting the tick „Temperature dependent „, we assign the capacitance a temperature model „CMODEL“, with TC1=0.001 by default. The parameter TC1 may be changed in the library „spice.lib“.

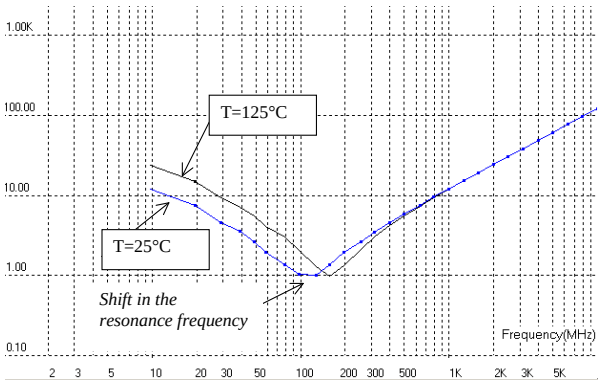


Figure 13: study of the impedance variation with frequency, for two different temperatures (capa_var_temp.sch)

The simulation of figure 13 has been performed for TC1=-0.005 (quite a big temperature dependence), by storing the result of a first simulation using T=25℃ (in blue) and then a second simulation for T=125℃ (in black). As expected, the capacitance decrease with temperature provokes a shift of the resonant frequency from 100MHz to 150MHz.

References

[1] E. Sicard, S. Ben Dhia “Basic CMOS cell design”, McGraw Hill, 450 pages, international edition 2007 – ISBN 9780071488396

[2] W. Liu "Mosfet Models for SPICE simulation including Bsim3v3 and BSIM4", Wiley & Sons, 2001, ISBN 0-471-39697-4