EMC Problem
Immunity of the reset line of a digital IC

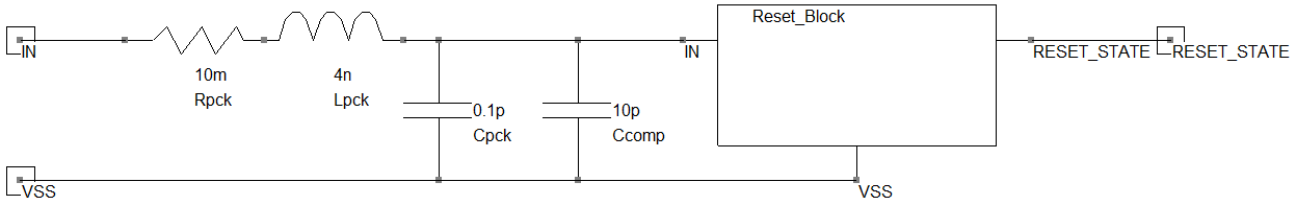
This problem is focused on the evaluation of the susceptibility of the reset input of a microcontroller. We consider a microcontroller, mounted on a four-layer FR4 board, whose reset line is pulled-up normally to the 3.3 V power-supply plane of the board by a 1 kΩ resistor. The decoupling of the power supply plane is supposed ideal. The reset of the microcontroller is triggered when a user button pulls down this input to a voltage lower than 1.65 V. The reset input buffer is fast enough to respond to pulse duration of 0.3 ns. The IC pad can withstand maximum voltage of +/- 10 V.

On the studied application board, the reset line is routed on the top layer, at 0.38 mm of a ground plane. The length of the PCB trace, which connects the reset input, the pull-up resistor and the button is 50 mm long. Its width is 0.15 mm. This line is not routed outside the board and end-user cannot have direct contact with it.

The application board has to comply with two susceptibility-related requirements:

- radiated susceptibility: the application must operate without loss of functionality when it is illuminated with a continuous wave (CW) 100 V/m plane wave, between 80 MHz and 10 GHz.
- electrostatic discharge (ESD): the application must operate without loss of functionality when direct contact +/- 4 kV ESD are applied only on exposed terminals. The ESD pulse complies with IEC61000-4-2 standard.

The electrical equivalent model of the reset input is shown here ('model_reset_input.sch'). C_{comp} is the equivalent input capacitance of the IC terminal. R, L, C model the input package effect. The block Reset_Block models the digital operation of the reset input. If a voltage less than 1.65 V is applied on the Reset_Block input during at least 0.3 ns, the pin RESET_STATE is set to 1 V.



1. Is the Reset pin critical for the functional safety of the application ? At first sight, is this pin exposed to electromagnetic disturbance risks in this application ?

2. Firstly, the radiated susceptibility of the reset line is investigated.

a. Propose an equivalent electrical model of the reset line, including the pull-up resistor and the equivalent input impedance of the reset input buffer. The effect of the PCB trace can be neglected in this part.

b. Modify the previous model to include the effect of the plane wave illumination.

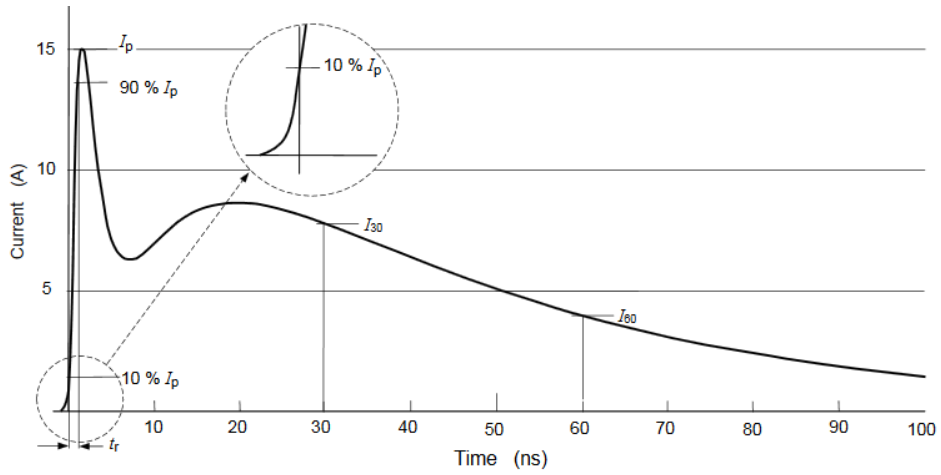
c. Estimate the worst-case voltage induced on the reset input at the following frequency: 100 MHz, 300 MHz, 1 GHz, 3 GHz and 10 GHz.

d. Conclude about the radiated susceptibility of the reset input.

e. If a failure risk exists, what simple suggestion(s) could you propose to reduce the radiated susceptibility ?

Secondly, the susceptibility to ESD is investigated. Even if the reset input is not exposed to direct contact ESD, the reset line is routed in close proximity of a digital RX line, which is connected to a cable harness through a connector and, thus, exposed to ESD. Both lines have the same dimensions. They are routed in parallel along almost 50 mm and are separated by 0.3 mm.

To test the susceptibility of electronic devices to ESD, a ESD stimulator, called ESD gun, is used. An equivalent model is given by the model 'model_gun.sch'. The transient profile of the current delivered by the ESD gun on a 2 Ω load must comply to the following standard waveform given by the following figure.



Ideal contact discharge current waveform at 4 kV (2 ohms) according to IEC61000-4-2

Table 3 – Contact discharge current waveform parameters

Level	Indicated voltage kV	First peak current of discharge ±15 % A	Rise time t_r (±25 %) ns	Current (±30 %) at 30 ns A	Current (±30 %) at 60 ns A
1	2	7,5	0,8	4	2
2	4	15	0,8	8	4
3	6	22,5	0,8	12	6
4	8	30	0,8	16	8
The reference point for measuring the time for the current at 30 ns and 60 ns is the instant when the current first reaches 10 % of the 1st peak of the discharge current. NOTE The rise time, t_r, is the time interval between 10 % and 90 % value of 1st peak current.					

3. Verify that the simulated current complies with IEC61000-4-2 standard.

4. With 'Interconnect Parameters' tools, build an equivalent model of the RX and reset traces.

4. The model of the RX input buffer is given in model_RX_input.sym. Build a model to simulate the voltage induced on reset trace terminals when a direct contact ESD is applied on RX input at the connector.

a. Simulate the voltages induced on reset trace terminals. Which effect(s) induces these voltages ?

b. Is a undesirable reset possible when a +/- 4 kV ESD is applied on RX input ? Is it a hard or a soft failure ?

c. What is the actual immunity level of the application to reset failure ?

5. Propose three general strategies to solve the ESD-induced reset failure.

6. What should be the minimum separation between RX and reset line (length of reset trace remains unchanged) to solve the ESD-induced reset failure ? Same question for the trace length if the separation is 0.3 mm) ?

7. Does a RC filter placement at reset input improve the immunity to ESD-induced reset failure ? Propose a couple of R-C value and simulate the effect.